

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O		GPI
37	PWM3/GPA3	/			GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0/GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	/	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4//GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSC#//GPD3	EXT_SC#	ECSC#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI


Pin	Pin Name	Signal Name	Type	Default
48	GPH0	VSUS_ON	O	L GPI
54	GPH1	VSUS_GD#	I	H GPI
55	GPH2	CPUPWR_GD#	I	H GPI
69	GPH3	PM_PWRBTN#	O	H GPI
70	GPH4	SUSC_ON	O	L GPI
75	GPH5	SUSB_ON	O	L GPI
76	GPH6	CPU_VRON	O	L GPI
105	GPH7	PM_RSMRST#	O	L GPI
148	GPI0	ICH7_PWROK	O	L GPI
149	GPI1	/	O	GPI
152	GPI2	MCHOK	I	L GPI
155	GPI3	CHG_EN#	O	H GPI
156	GPI4	PRECHG	O	L GPI
168	GPI5	BAT_LL#	O	H GPI
174	GPI6	BAT_LEARN	O	L GPI
93	ADC8	KID0	I	
94	ADC9	KID1	I	
101	DAC2	BL_PWM_DA	O	
102	DAC3	BATSEL_2P#	O	

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
Thermal Sensor	0100110X ( 98 )

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	O	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSPLPVR	PM_DPRSPLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PC#	STP_PC#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native



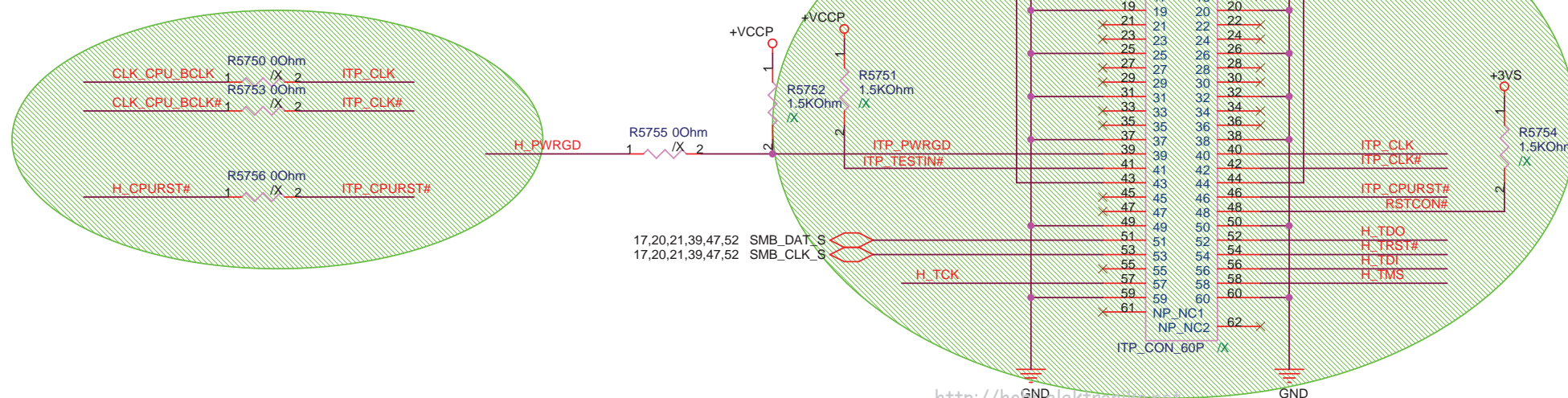
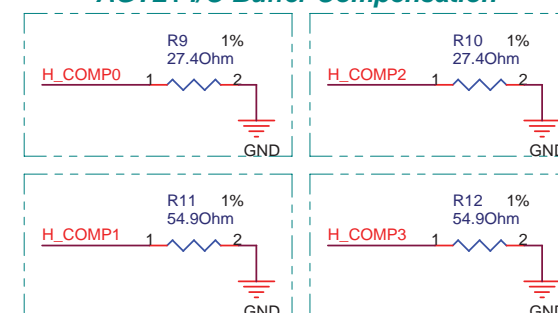
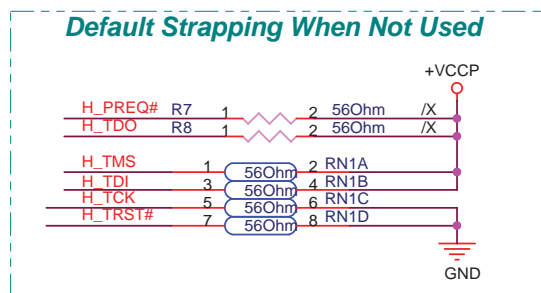
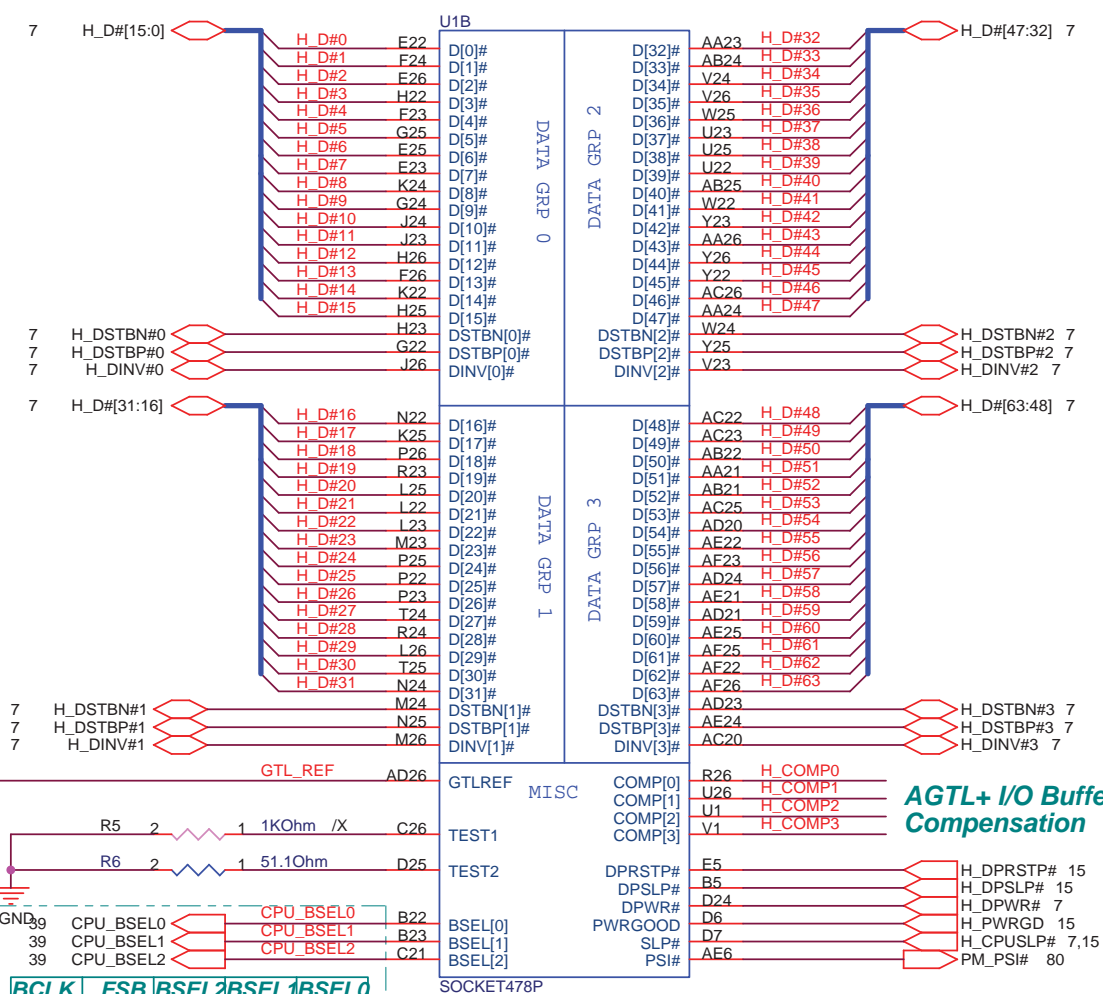
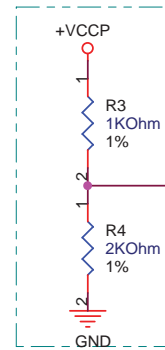
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ASUSTek Computer INC. Engineer: Alan Chu

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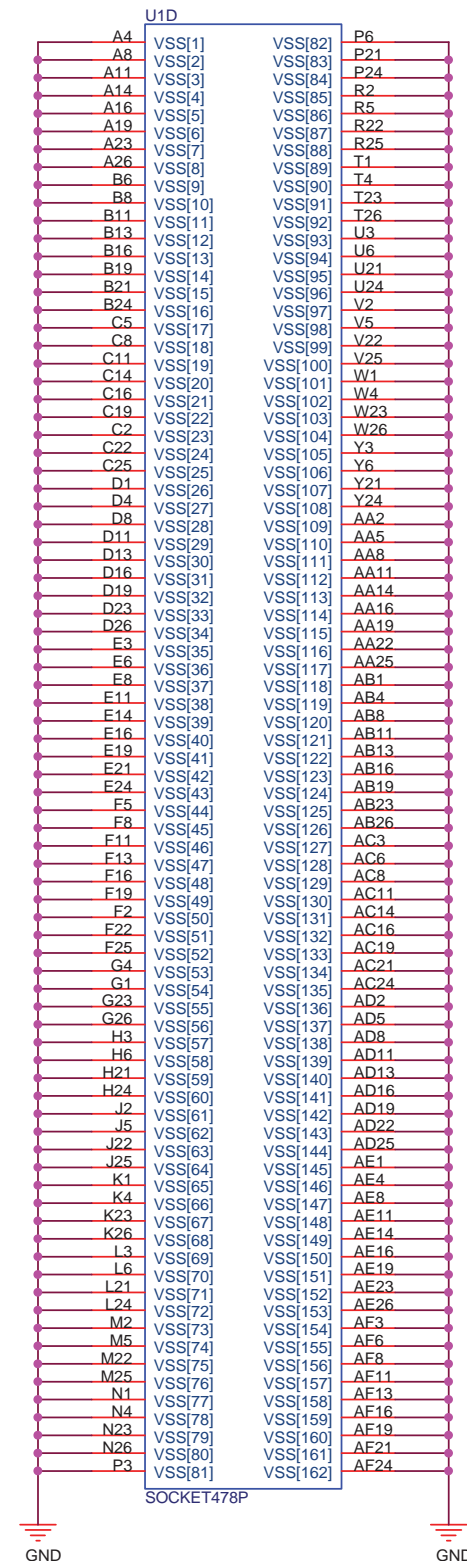
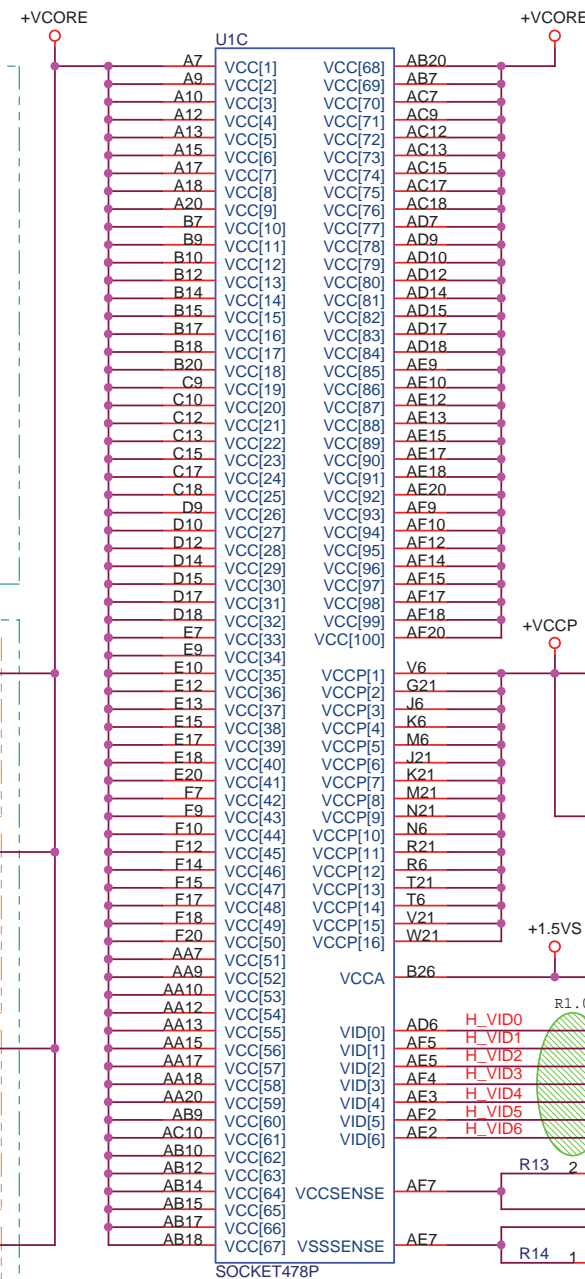
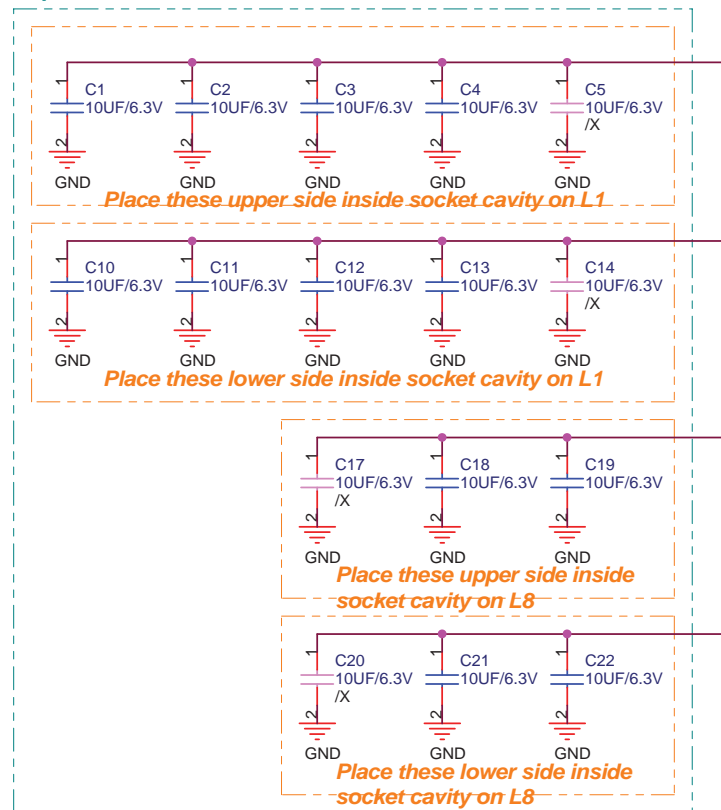


**CPU +VCORE  
Bulk-Decoupling  
Capacitors**

**CPU +VCORE  
Mid-Frequency  
Capacitors**

**CPU +VCCP  
Decoupling  
Capacitors**

**CPU +VCCA  
Decoupling  
Capacitors**



**+VCCP Decoupling Capacitor**  
Intel: 220UF \*1, 0.1UF \*4  
R1F: 220UF \*1, 0.1UF \*4



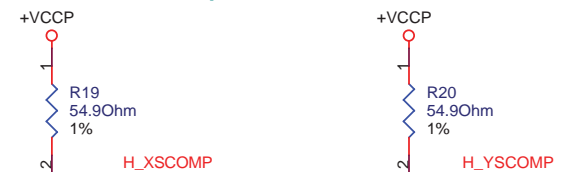
### RCOMP

For Calibrating the FSB I/O Buffer



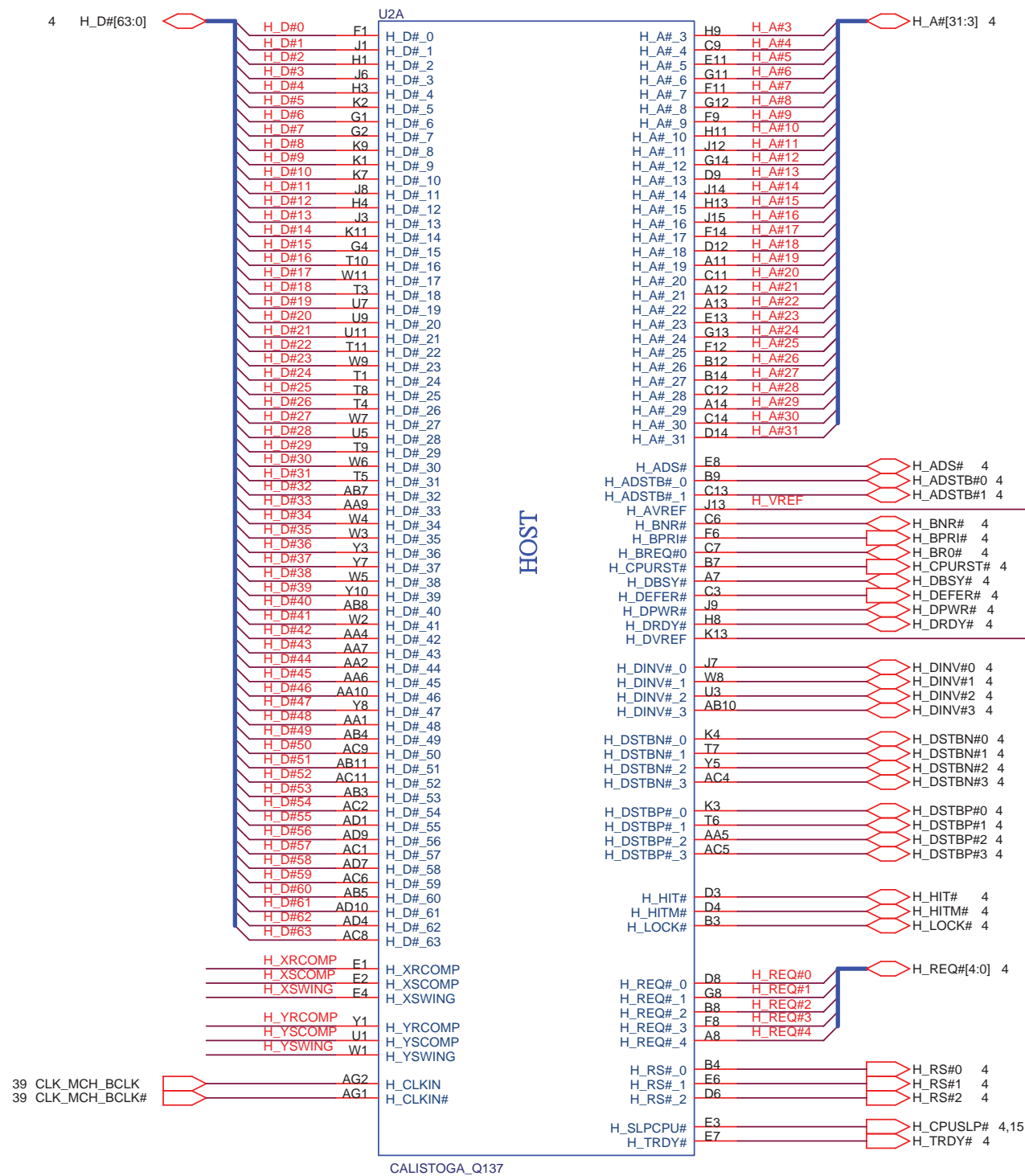
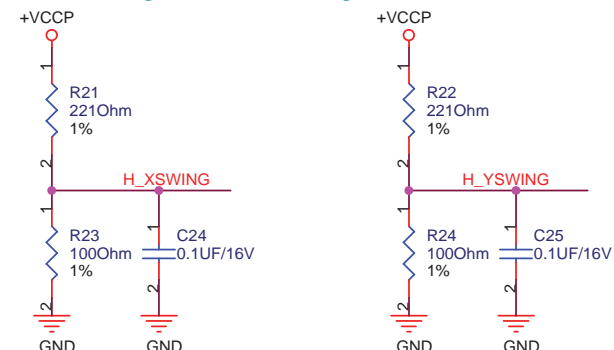
### SCOMP

For Slew Rate Compenssation on the FSB



### Voltage Swing

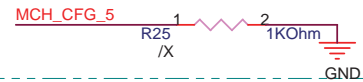
For Providing a Reference Voltage to The FSB RCOMP circuits



## GMCH Strapping

### CFG5 : DMI Strap

0 = DMI x2  
1 = DMI x4 (D)

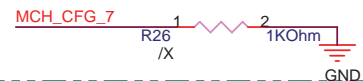


### CFG[13:12] : GMCH Test Mode

00 = Partial CLK Gating Disable  
01 = XOR Mode Enable  
10 = All Z Mode Enable  
11 = Normal Operation (D)

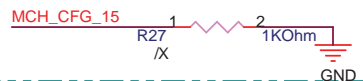
### CFG7 : CPU Strap

0 = DT/Transpotable CPU  
1 = Mobile CPU (D)



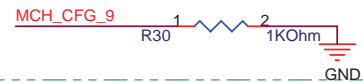
### CFG15 : ICH RESET Disable

0 = ICH Reset Disable  
1 = Normal Operation (D)



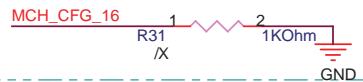
### CFG9 : PCIE Graphic Lane

0 = Reverse Lane  
1 = Normal Operation (D)



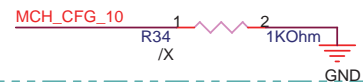
### CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable  
1 = Dynamic ODT Enable (D)



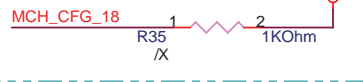
### CFG10 : HOST PLL VCO Select

0 = Reserved  
1 = Mobility (D)



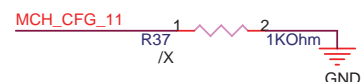
### CFG18 : VCC Select

0 = 1.05V (D)  
1 = 1.5V



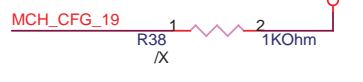
### CFG11 : PSB 4x CLK Enable

0 = 4x Enable  
1 = 8x Enable (D)



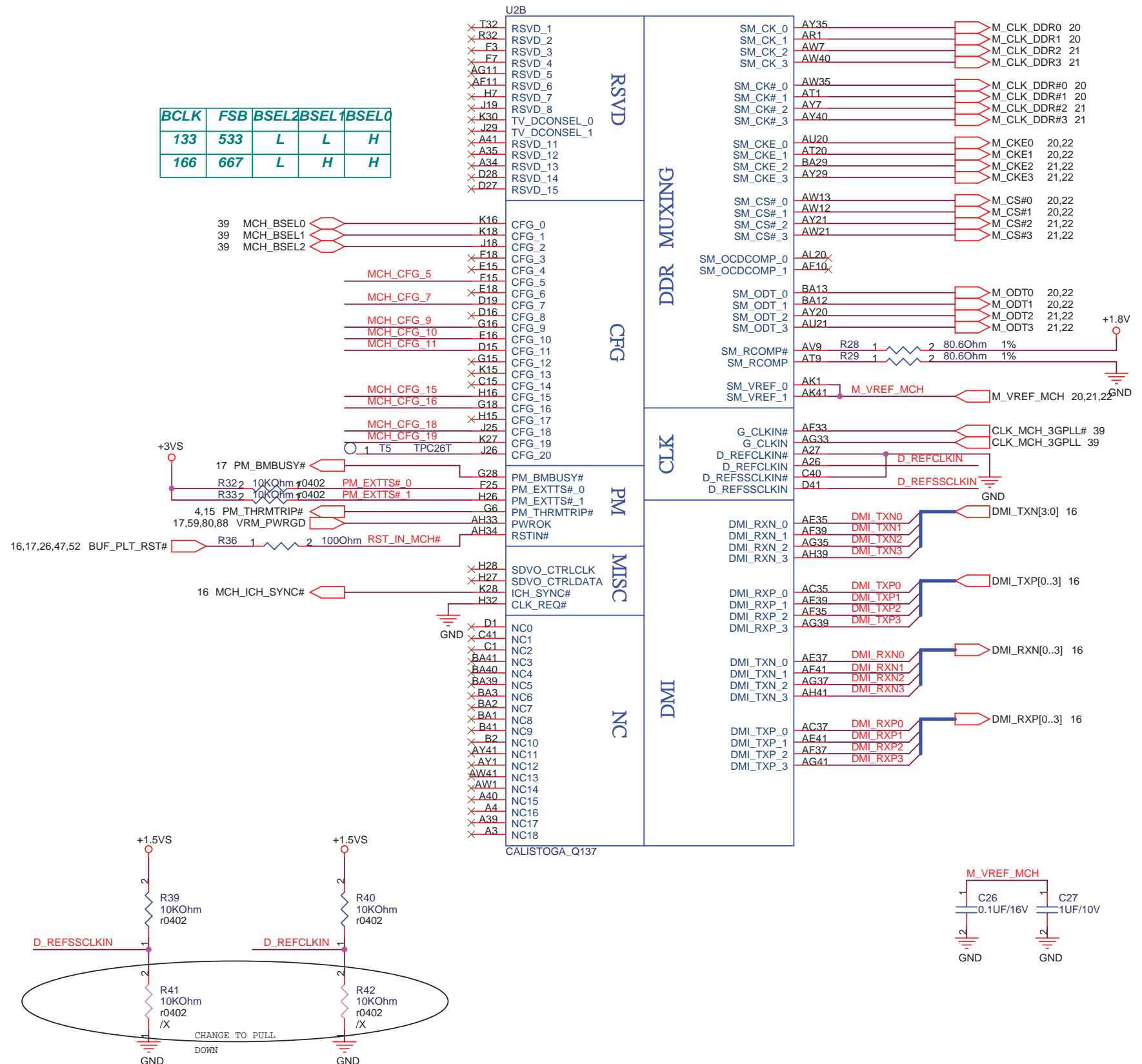
### CFG19 : DMI Lane Reversal

0 = Normal Operation (D)  
1 = Lanes Reversed

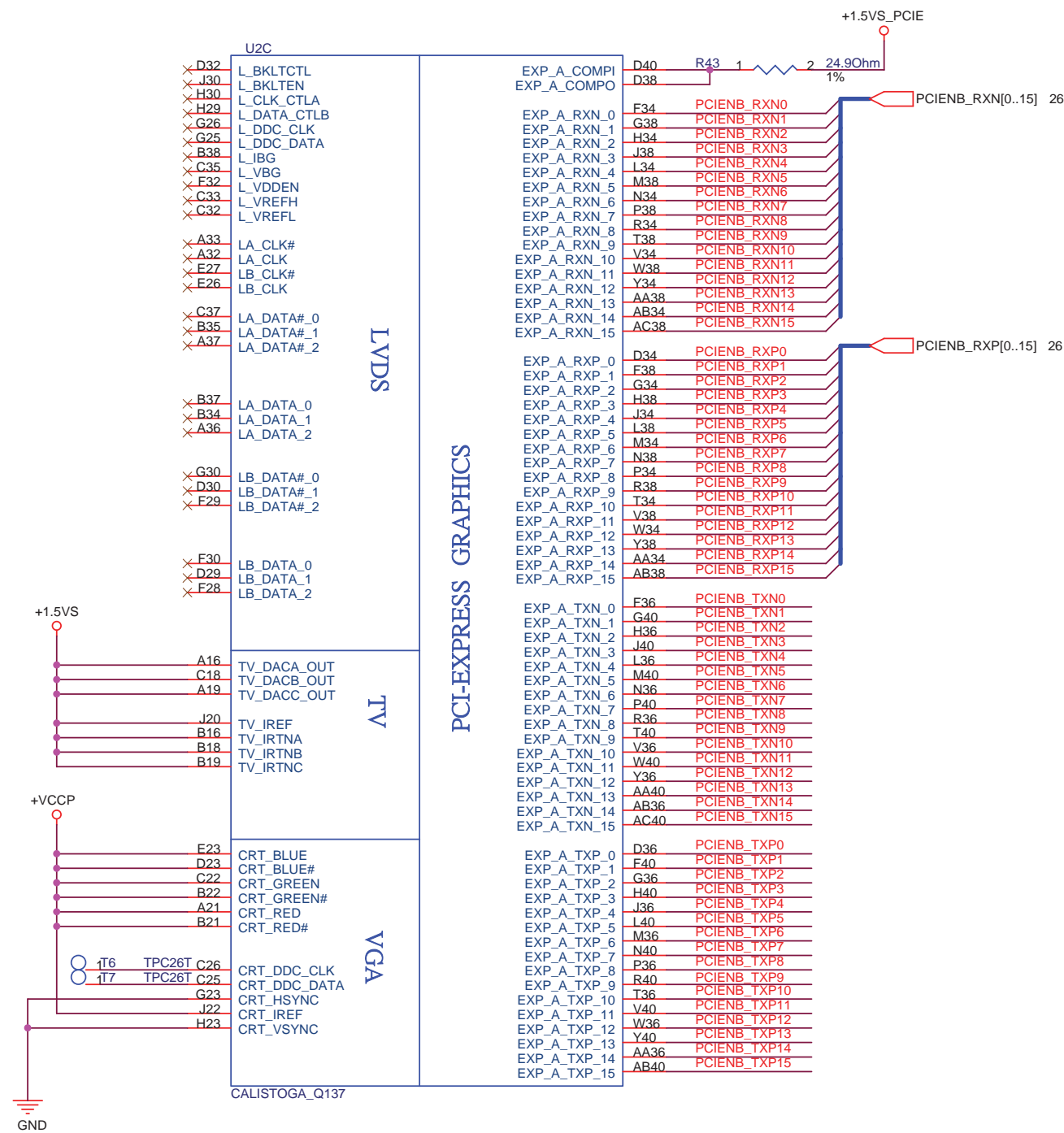


Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

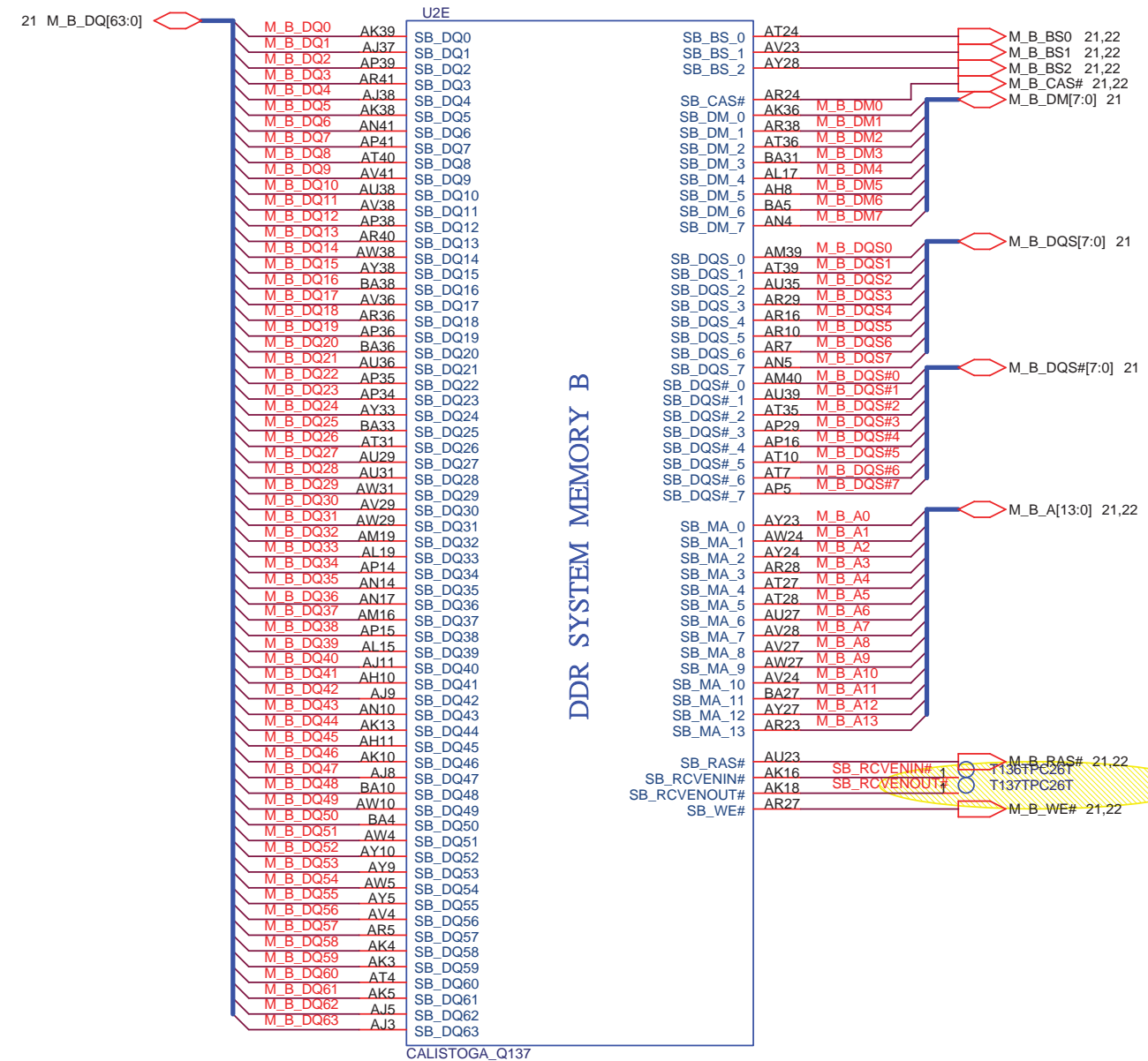
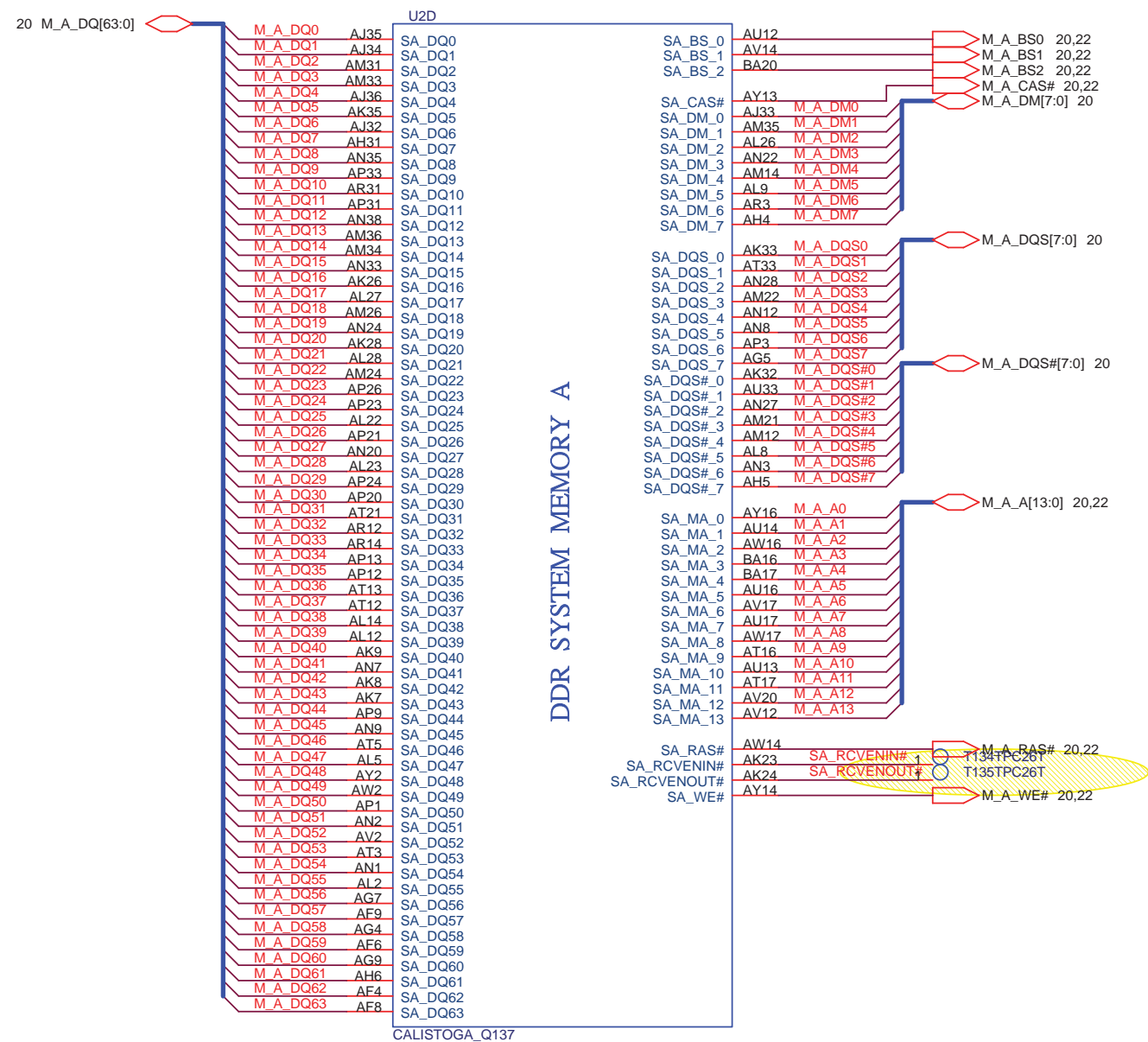
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

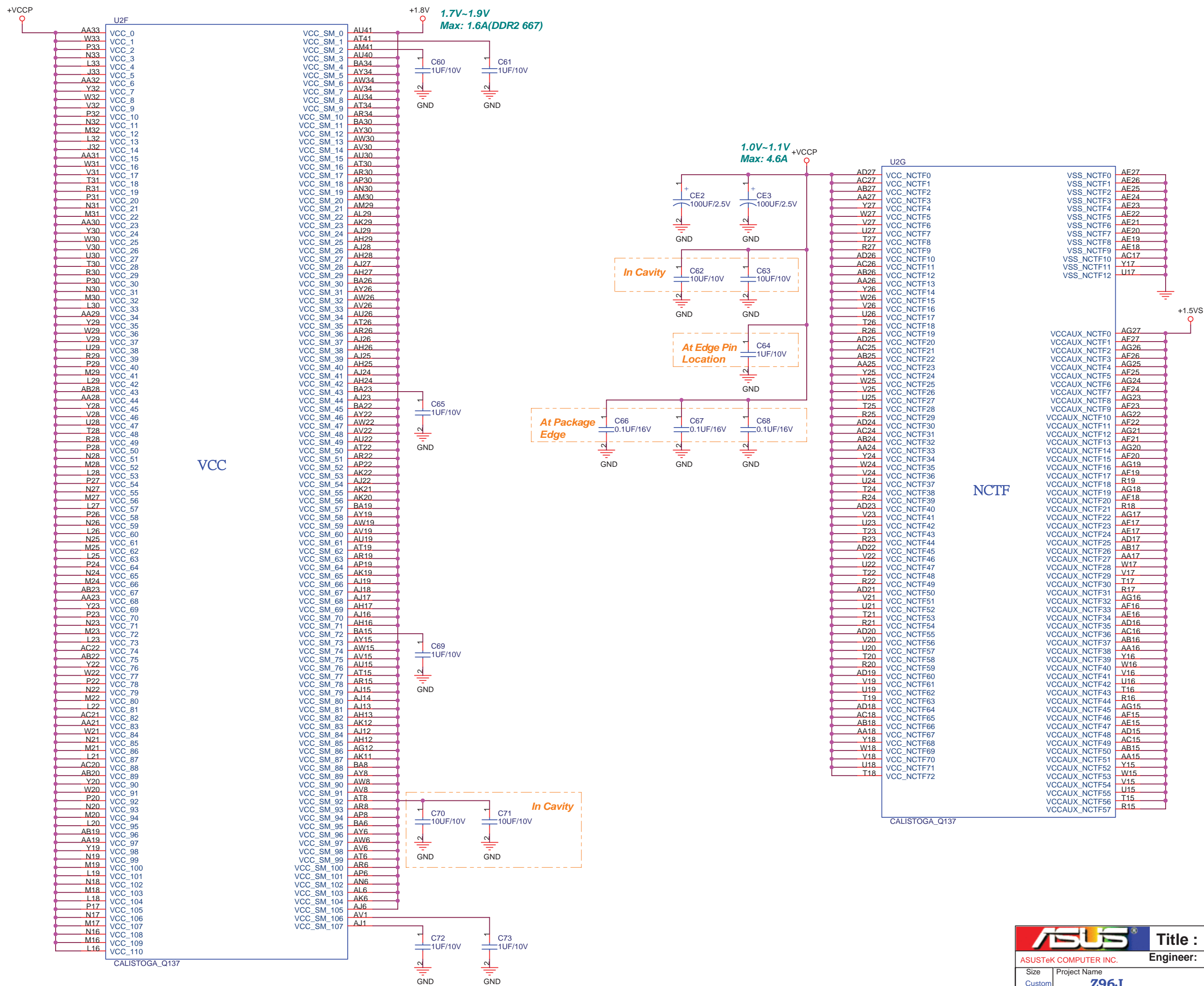






PCIEB_TXP15	1	2	PCIEG_RXP15	26
PCIEB_TXP14	C28	0.1UF/16V	PCIEG_RXP14	
PCIEB_TXP13	1	2 C29	PCIEG_RXP13	
PCIEB_TXP12	C30	0.1UF/16V	PCIEG_RXP12	
PCIEB_TXP11	1	2 C31	PCIEG_RXP11	
PCIEB_TXP10	C32	0.1UF/16V	PCIEG_RXP10	
PCIEB_TXP9	1	2 C33	PCIEG_RXP9	
PCIEB_TXP8	C34	0.1UF/16V	PCIEG_RXP8	
PCIEB_TXP7	1	2 C35	PCIEG_RXP7	
PCIEB_TXP6	C36	0.1UF/16V	PCIEG_RXP6	
PCIEB_TXP5	1	2 C37	PCIEG_RXP5	
PCIEB_TXP4	C38	0.1UF/16V	PCIEG_RXP4	
PCIEB_TXP3	1	2 C39	PCIEG_RXP3	
PCIEB_TXP2	C40	0.1UF/16V	PCIEG_RXP2	
PCIEB_TXP1	1	2 C41	PCIEG_RXP1	
PCIEB_TXP0	C42	0.1UF/16V	PCIEG_RXP0	
		C43	0.1UF/16V	
PCIEB_TXN15	1	2	PCIEG_RXN15	26
PCIEB_TXN14	C44	0.1UF/16V	PCIEG_RXN14	
PCIEB_TXN13	1	2 C45	PCIEG_RXN13	
PCIEB_TXN12	C46	0.1UF/16V	PCIEG_RXN12	
PCIEB_TXN11	1	2 C47	PCIEG_RXN11	
PCIEB_TXN10	C48	0.1UF/16V	PCIEG_RXN10	
PCIEB_TXN9	1	2 C49	PCIEG_RXN9	
PCIEB_TXN8	C50	0.1UF/16V	PCIEG_RXN8	
PCIEB_TXN7	1	2 C51	PCIEG_RXN7	
PCIEB_TXN6	C52	0.1UF/16V	PCIEG_RXN6	
PCIEB_TXN5	1	2 C53	PCIEG_RXN5	
PCIEB_TXN4	C54	0.1UF/16V	PCIEG_RXN4	
PCIEB_TXN3	1	2 C55	PCIEG_RXN3	
PCIEB_TXN2	C56	0.1UF/16V	PCIEG_RXN2	
PCIEB_TXN1	1	2 C57	PCIEG_RXN1	
PCIEB_TXN0	C58	0.1UF/16V	PCIEG_RXN0	
		C59	0.1UF/16V	





Title : NB-945PM(PWR)

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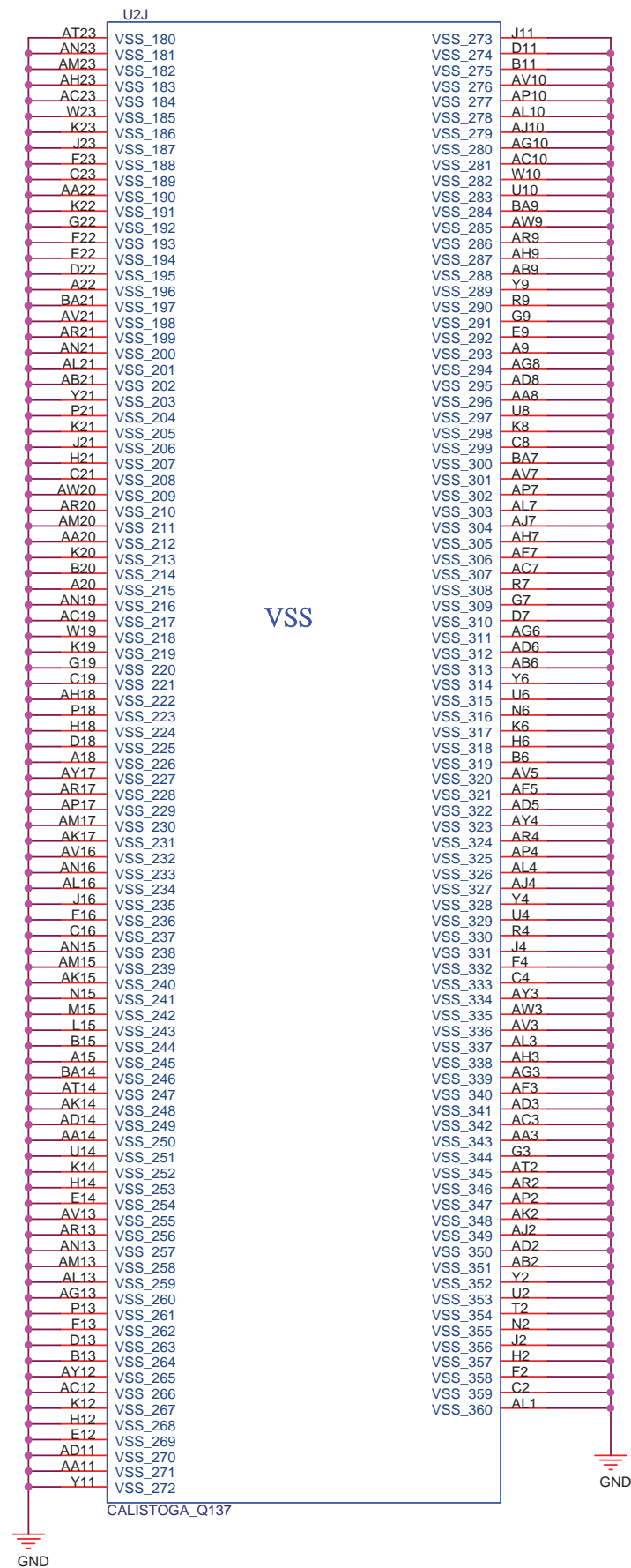
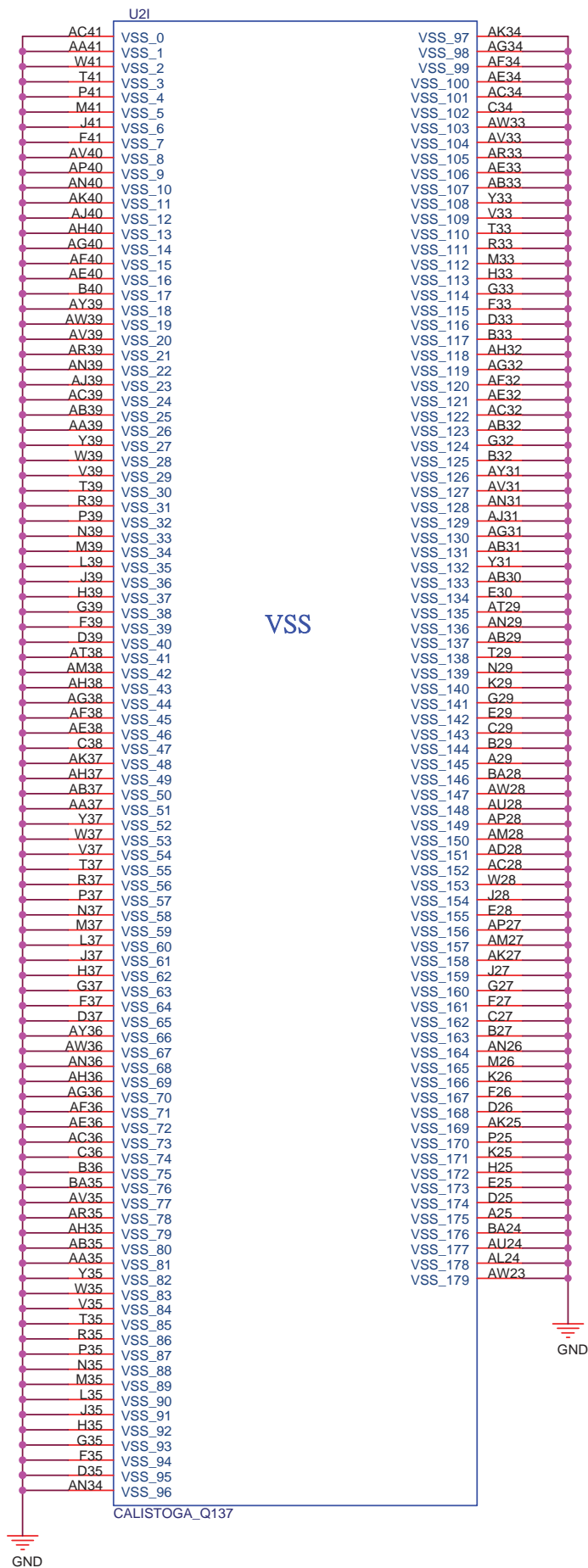
Engineer: Alan Chu

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Custom	296J	1.0

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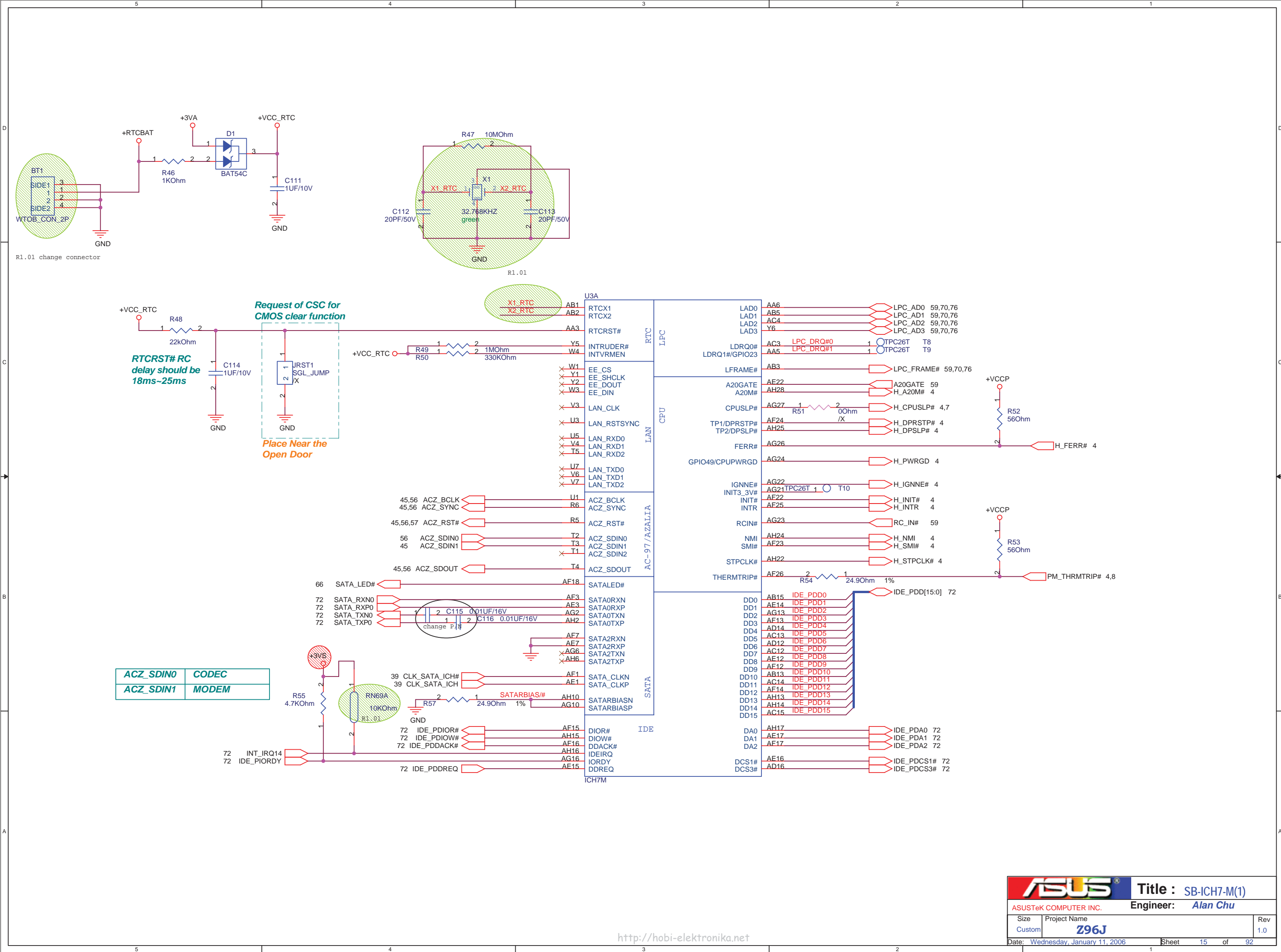


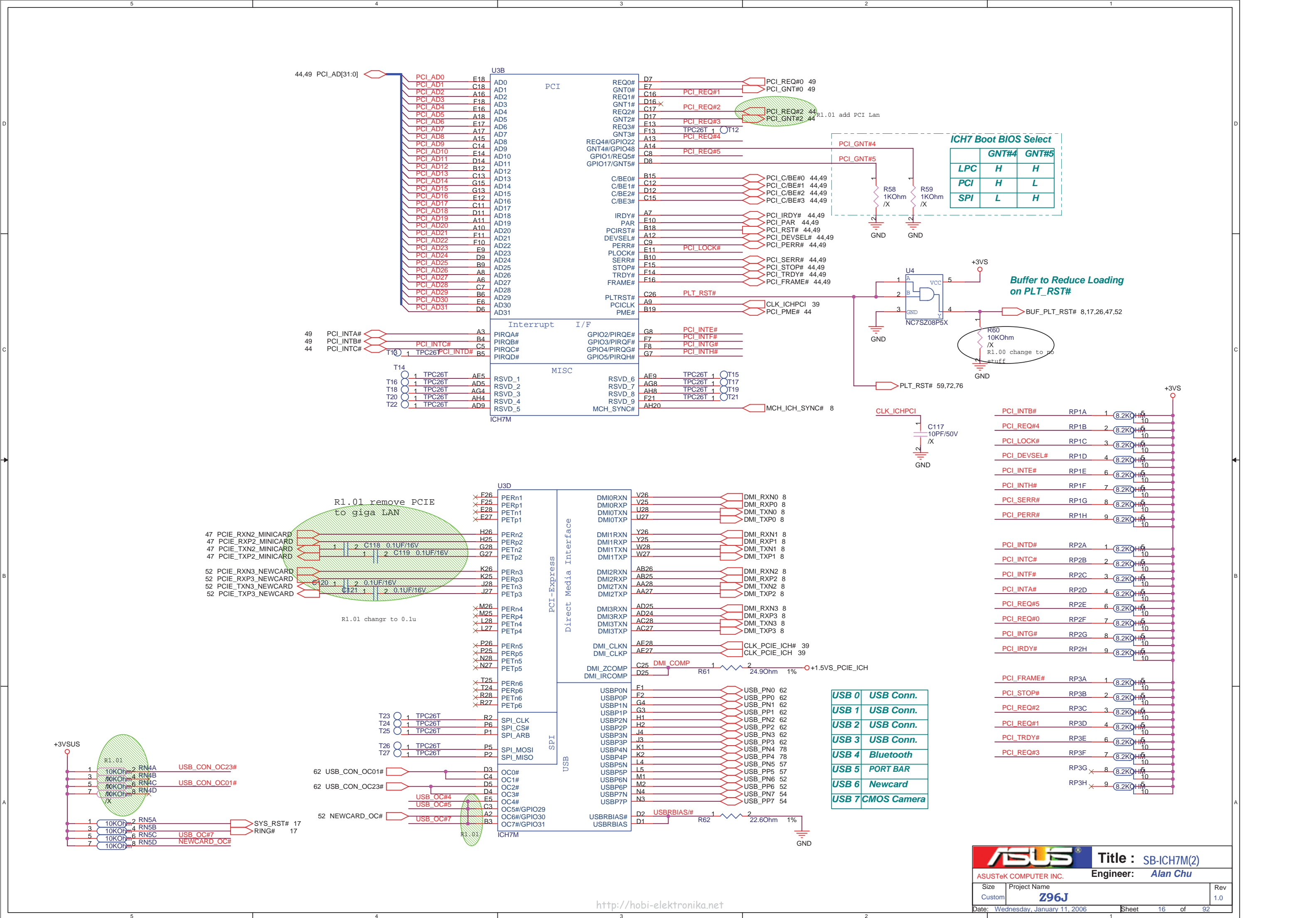




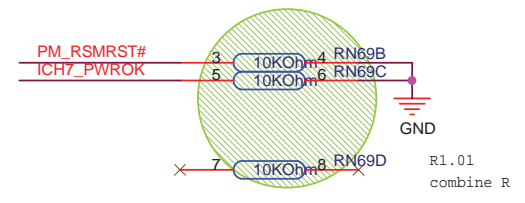
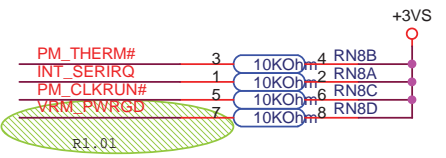
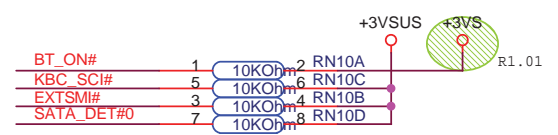
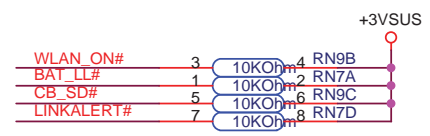
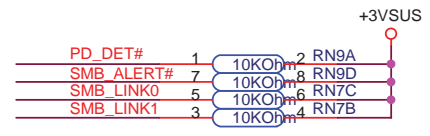
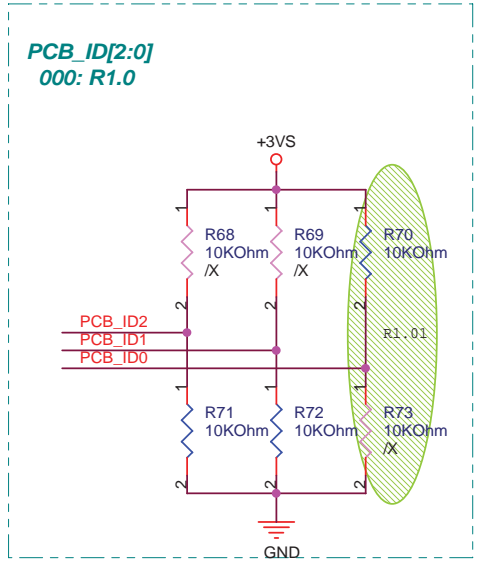
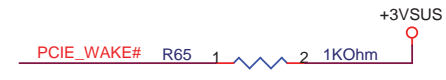
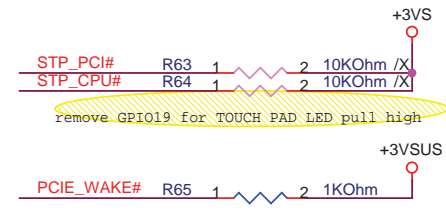
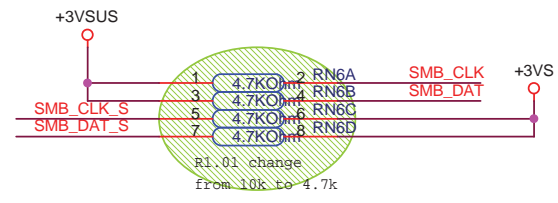
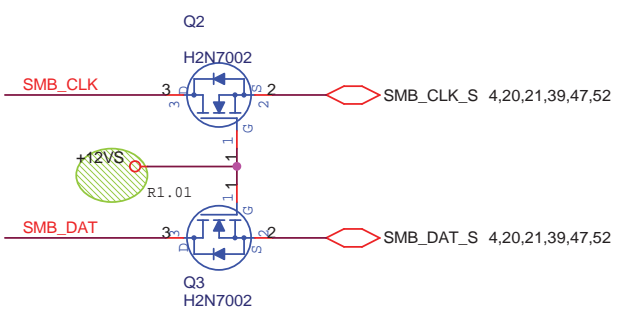
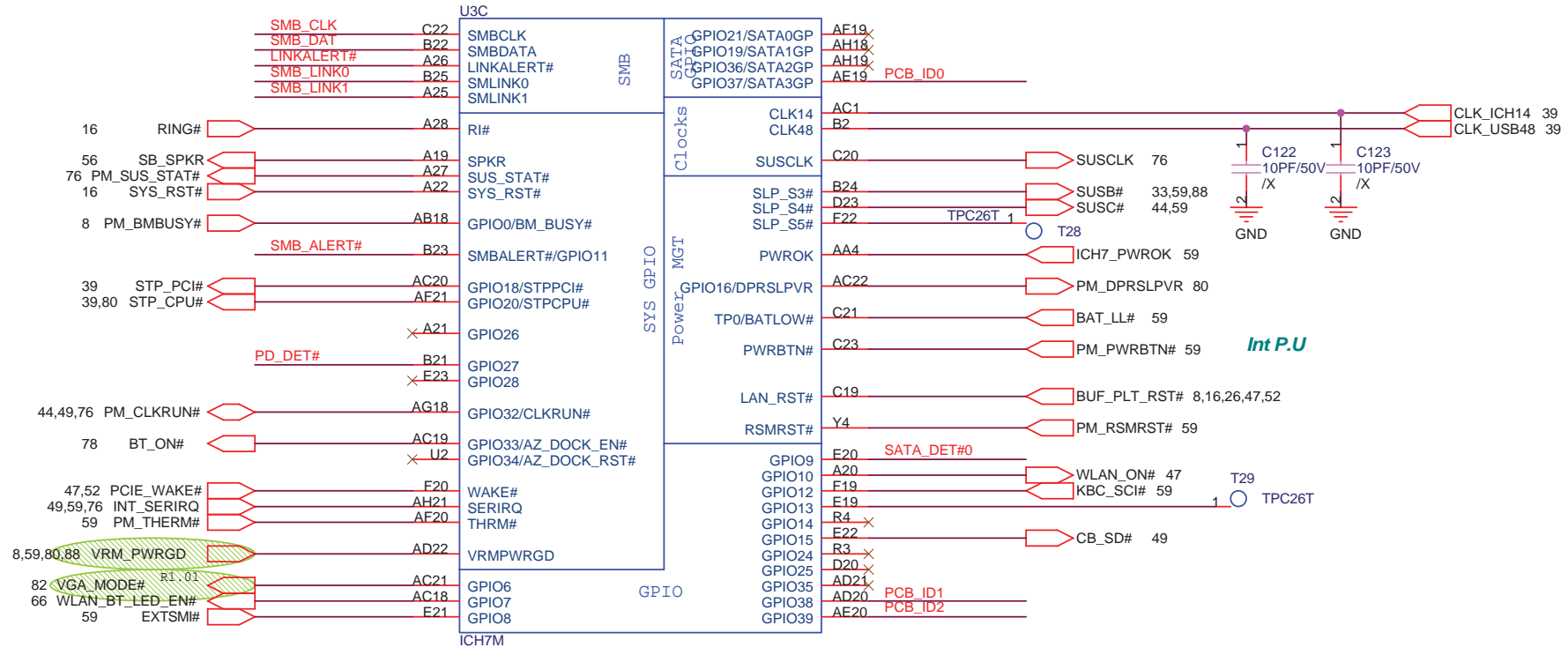








R1.01 add VGA mode select  
GPU\_VID = 1; Battery Mode ; +1.15V0 = 1.055V  
GPU\_VID = 0; Performance Mode ; +1.15V0 = 1.158V

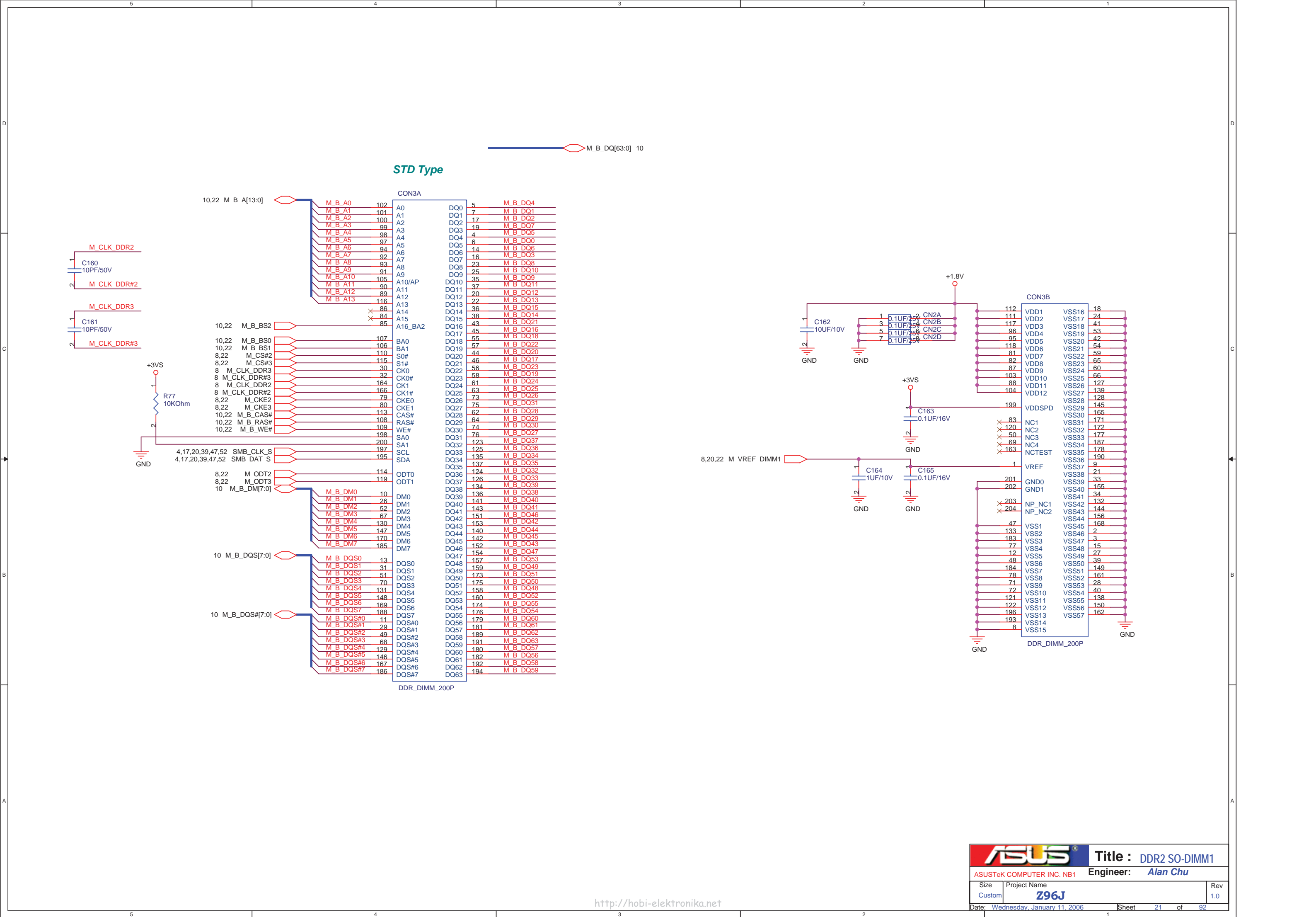


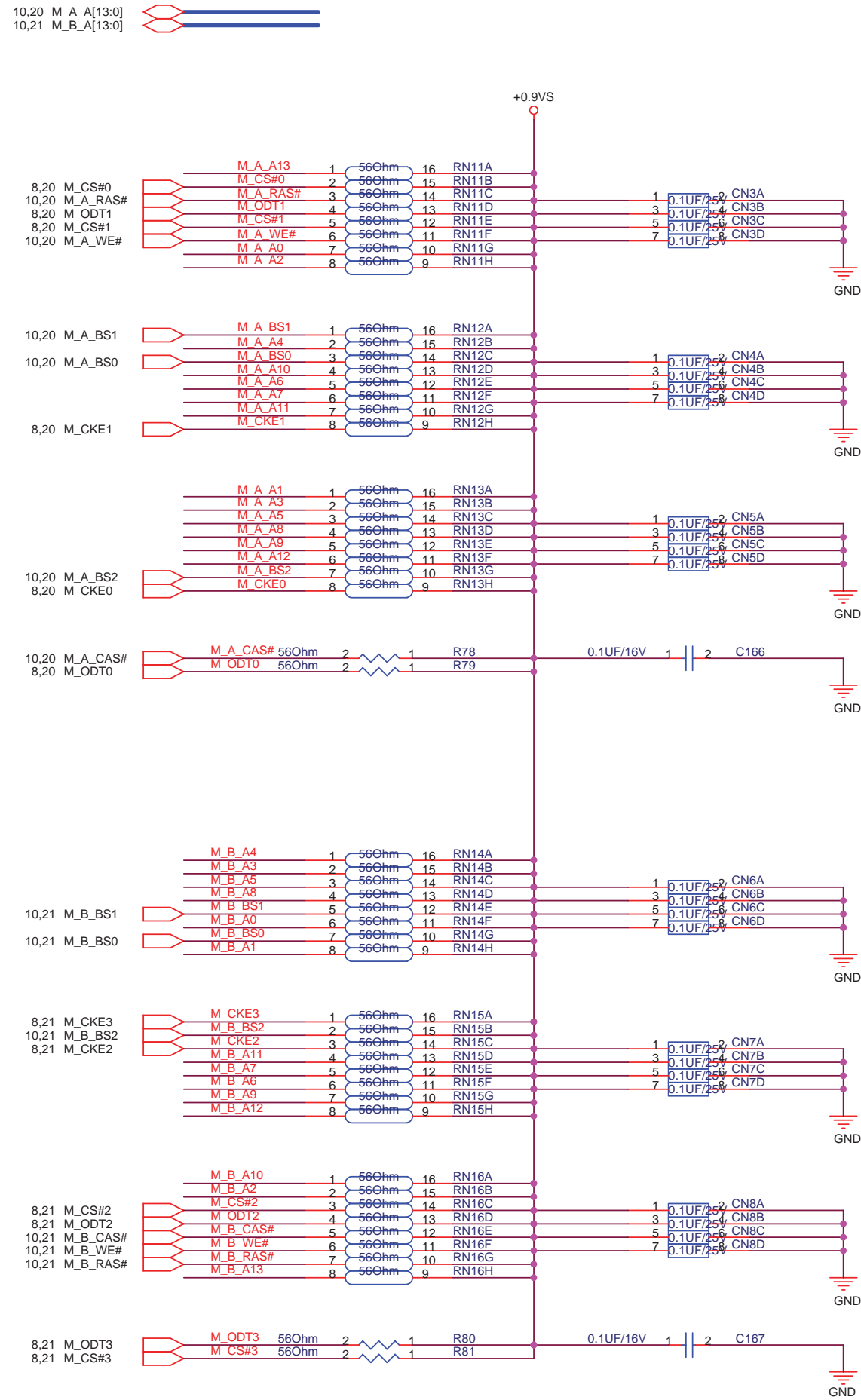
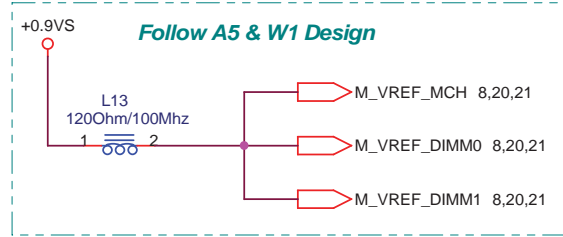








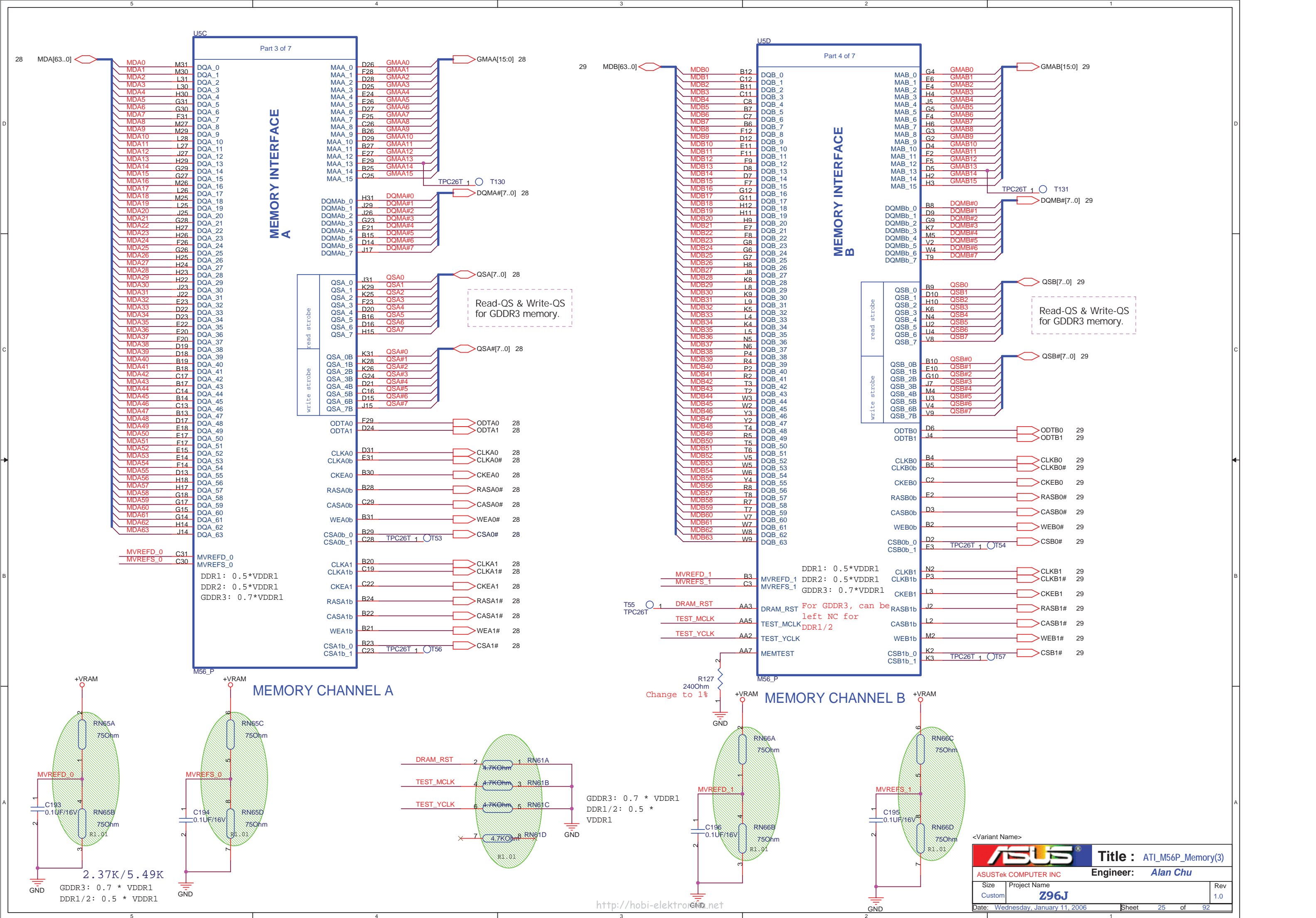






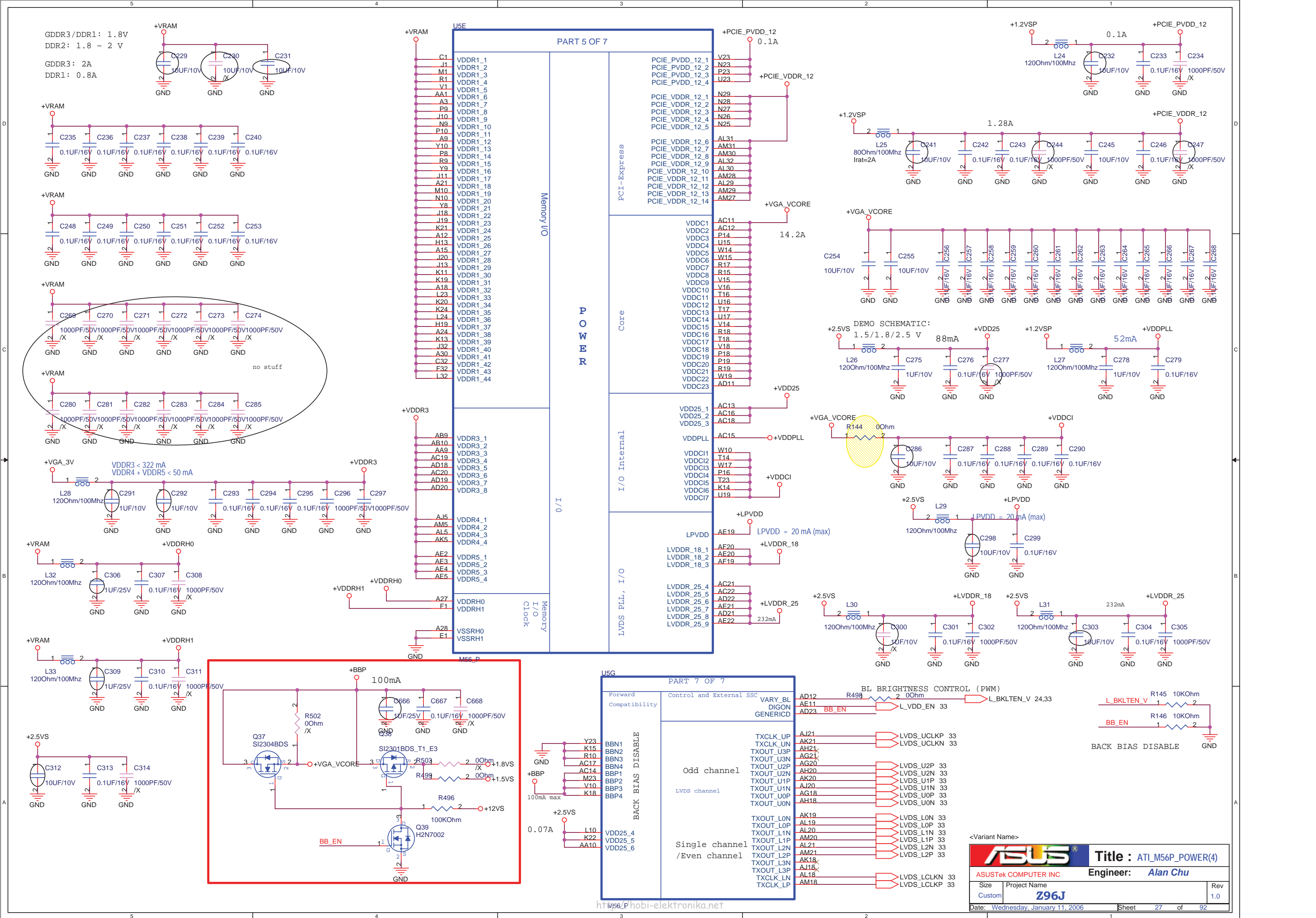










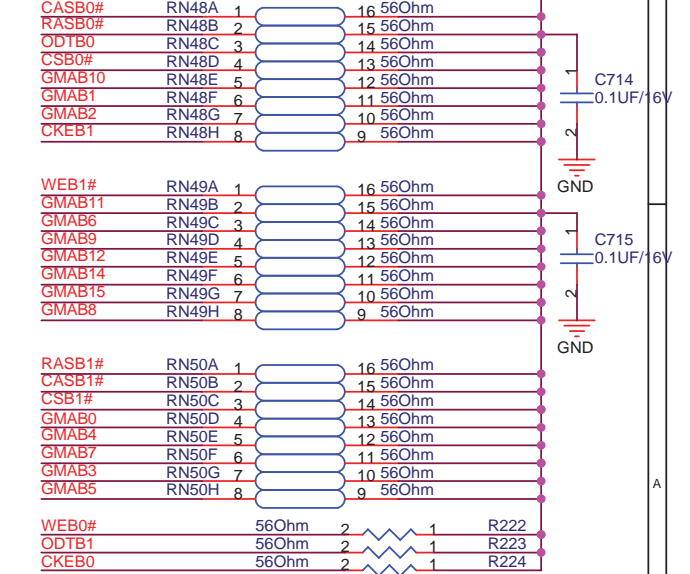
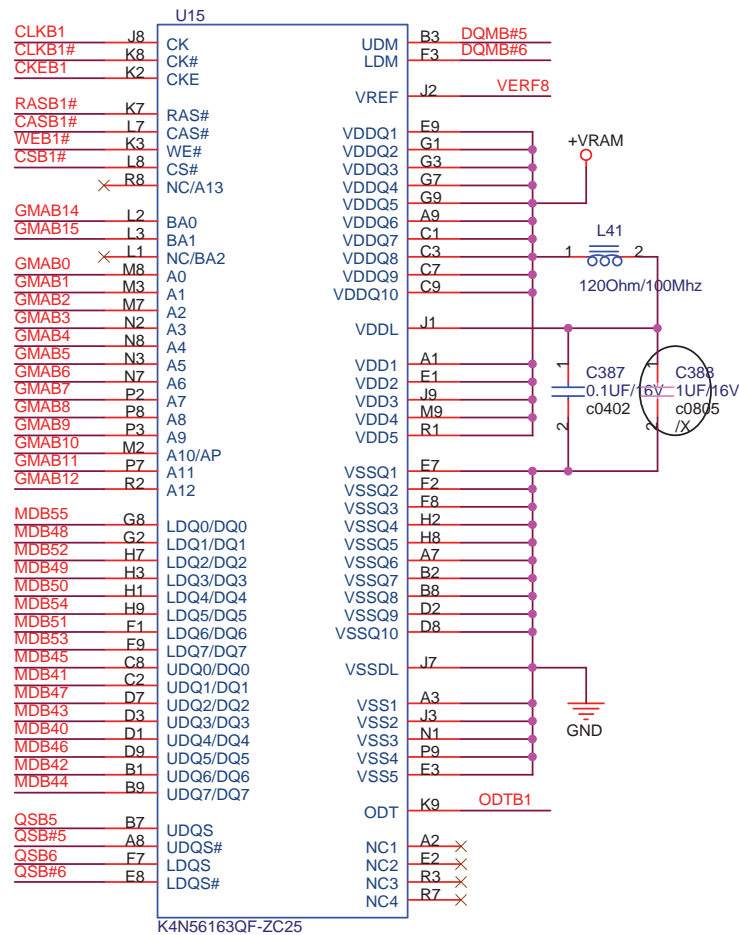
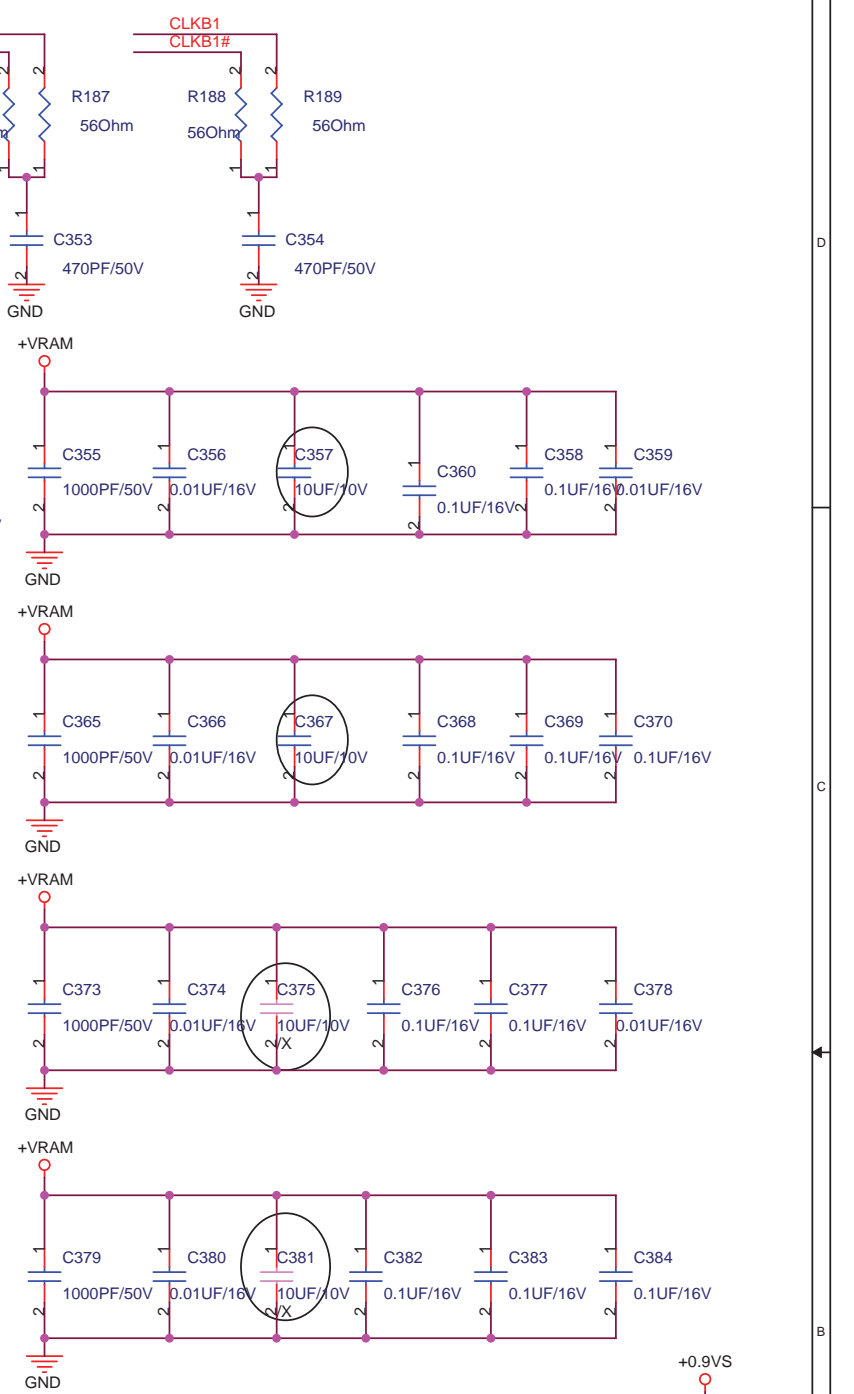
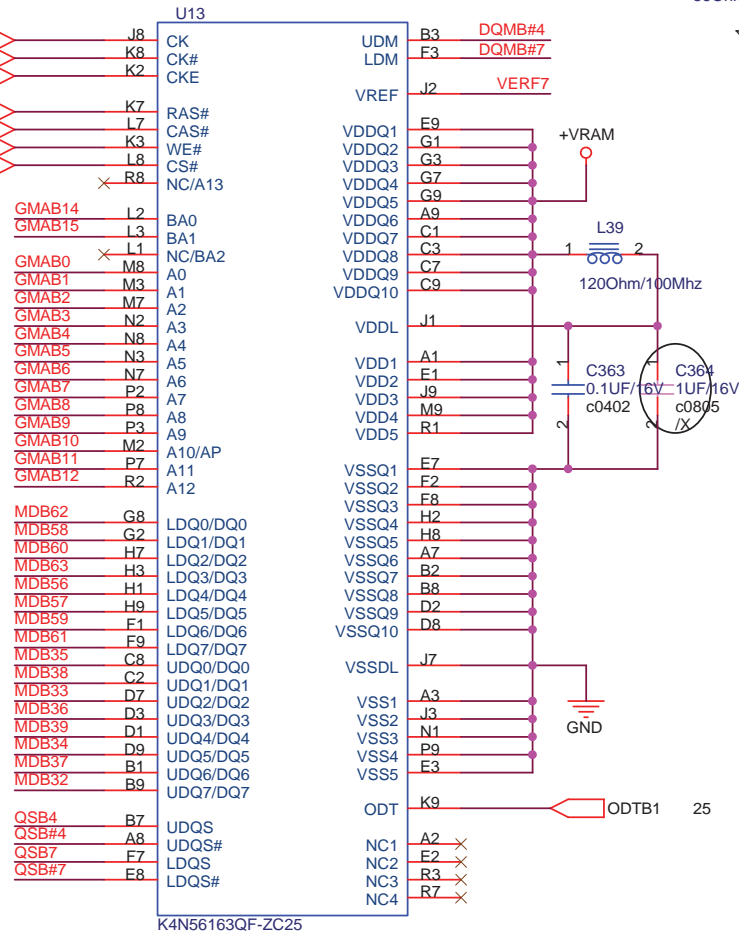
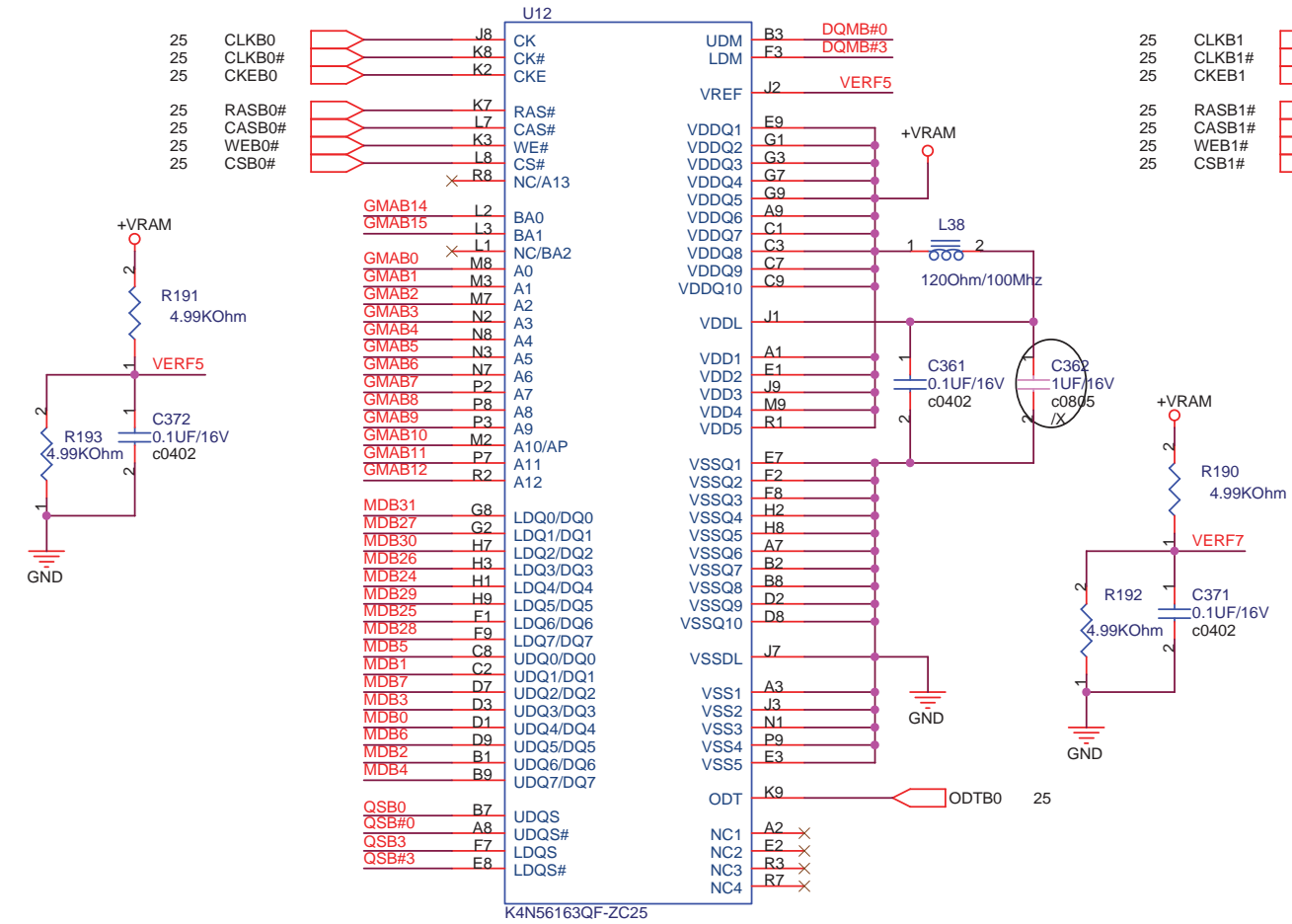






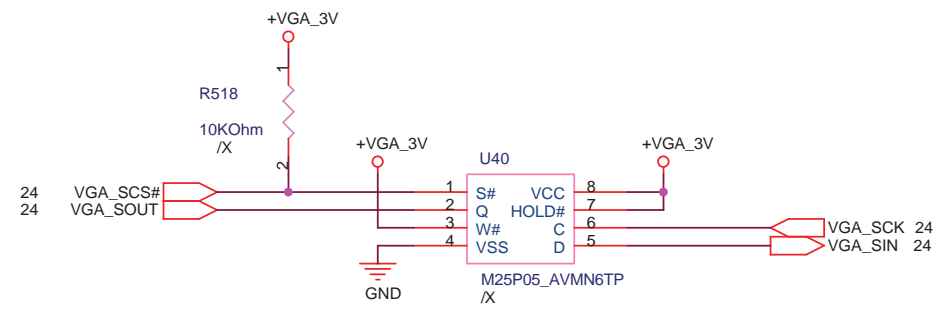
25 GMAB[15..0]  
25 QSB[7..0]  
25 QSB#7..0  
25 DQMB#7..0

MDB[31..0] 25  
MDB[63..32] 25

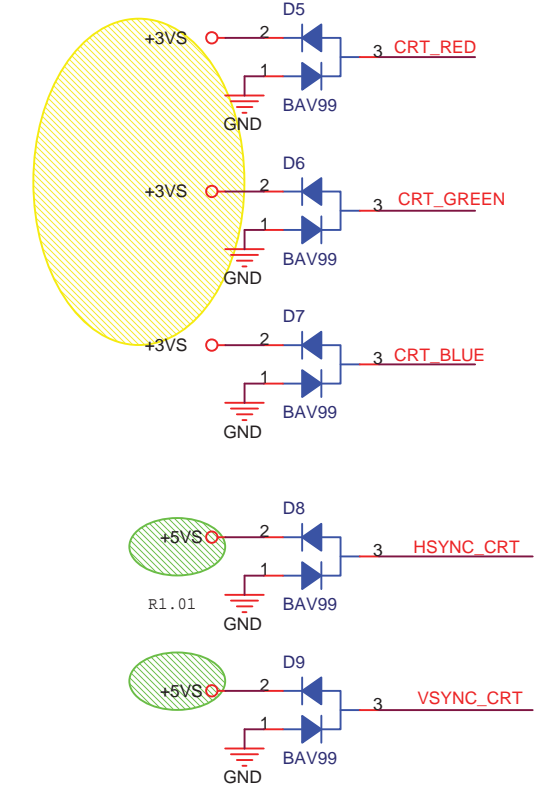
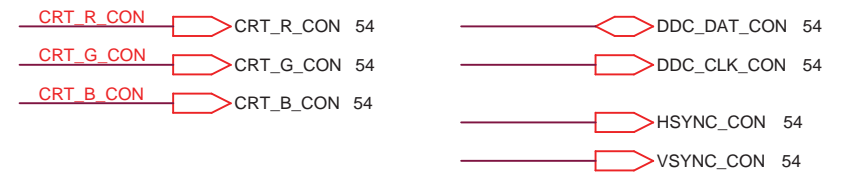
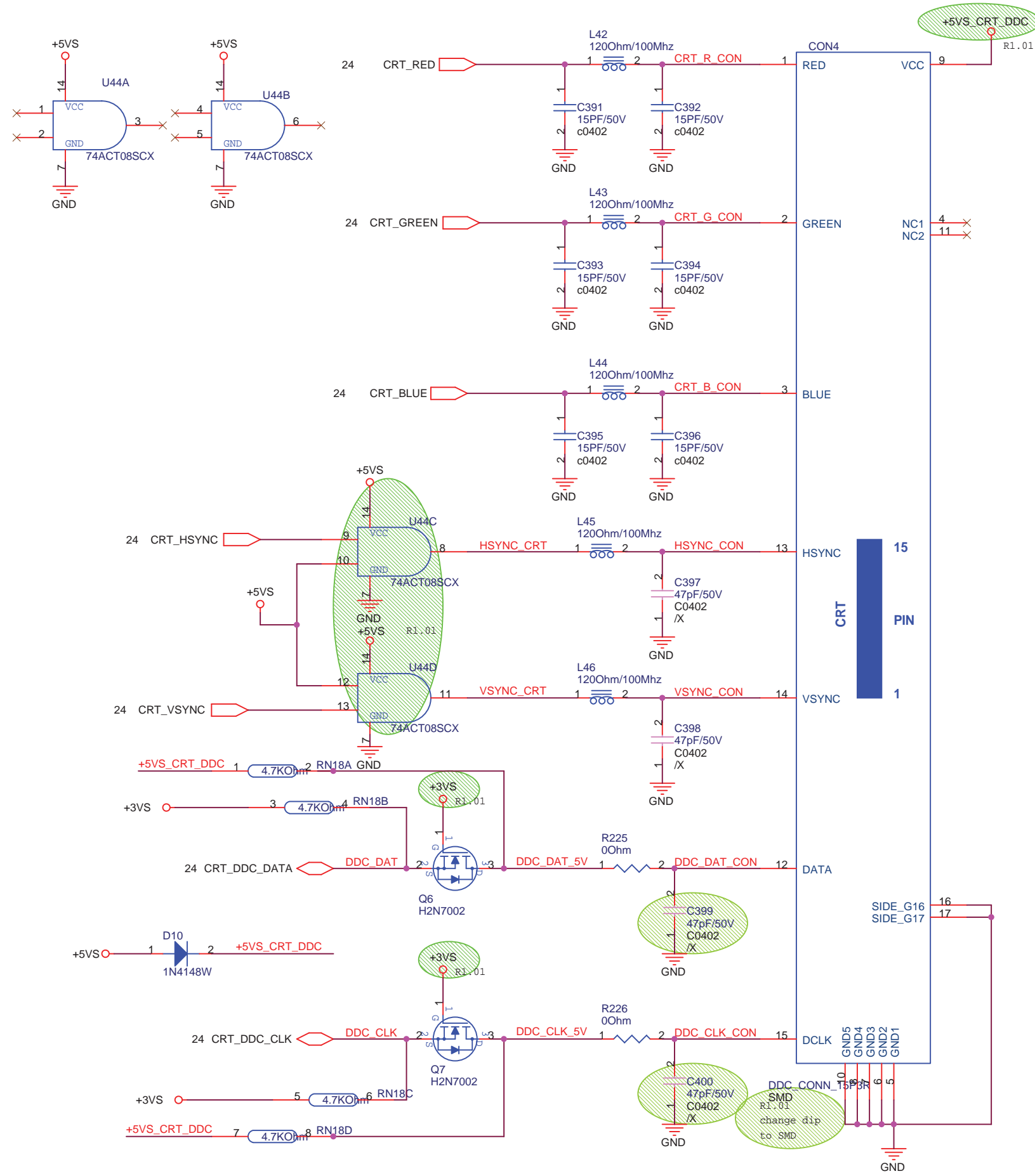


ASUS  
ASUSTek COMPUTER INC  
Size: Custom  
Project Name: Z96J  
Date: Wednesday, January 11, 2006

Title: ATL\_M56P\_VRAM\_B(6)  
Engineer: Alan Chu  
Rev: 1.0  
Sheet: 29 of 92



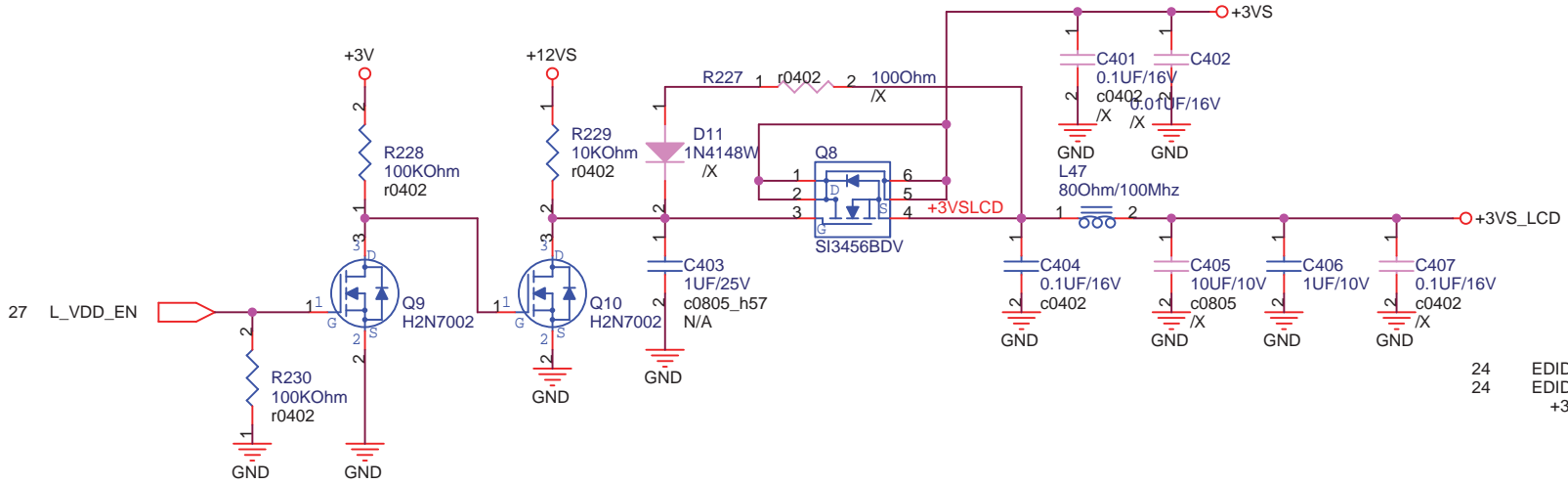




PLACE ESD Diodes near VGA port

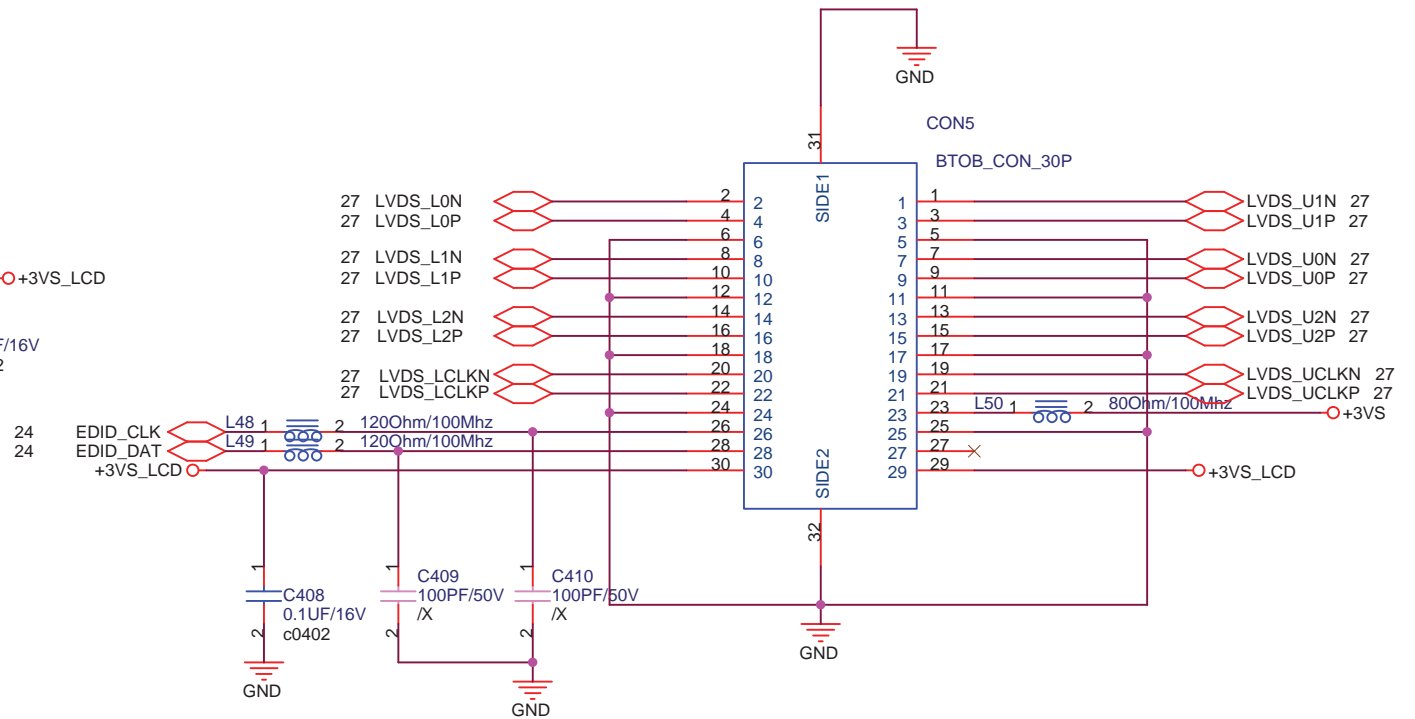
# LCD Backlight Control

## LCD Power



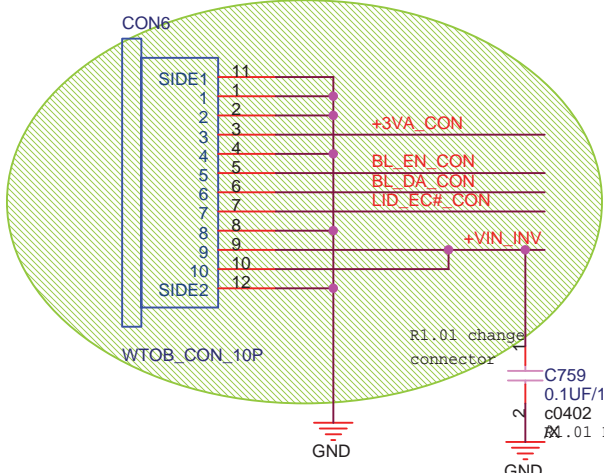
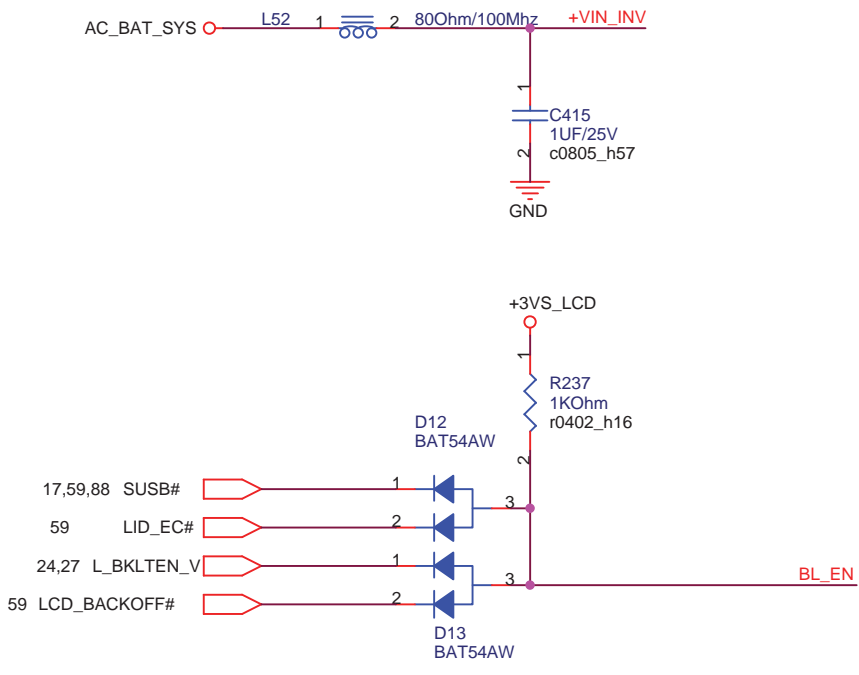
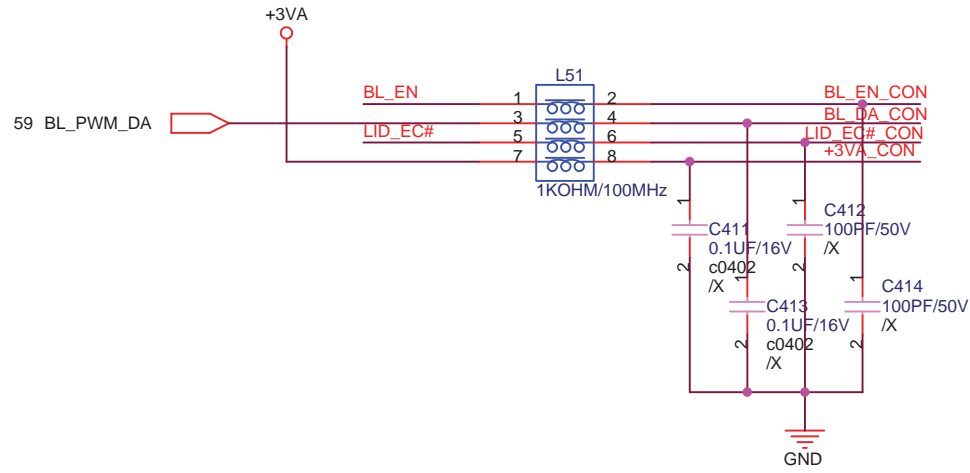
Cable Requirement:  
Impedence: 100 ohm +/- 10%  
Length Mismatch <= 10 mils  
Twisted Pair(Not Ribbon)  
Maximum Length <= 16"

# LCD LVDS Interface



## INVERTER Interface/Speaker CONN.

BIOS  
BACK\_OFF#:When user push "Fn+F7"  
button, BIOS active this pin to  
turn off back light.



R1.01 remove HW reserve pannel ID

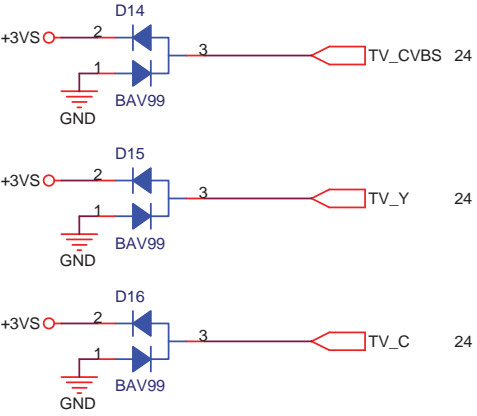
R1.01 change connector

ASUS		Title :LVDS & INVERTER	
ASUSTeK COMPUTER INC		Engineer: Alan Chu	
Size	Project Name	Rev	
Custom	Z96J	1.0	
Date: Wednesday, January 11, 2006	Sheet	33	of 92

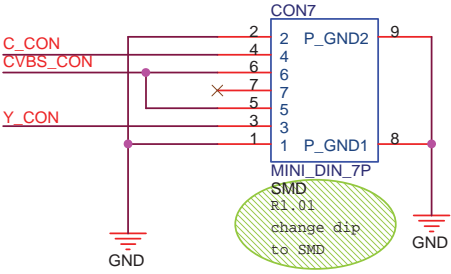
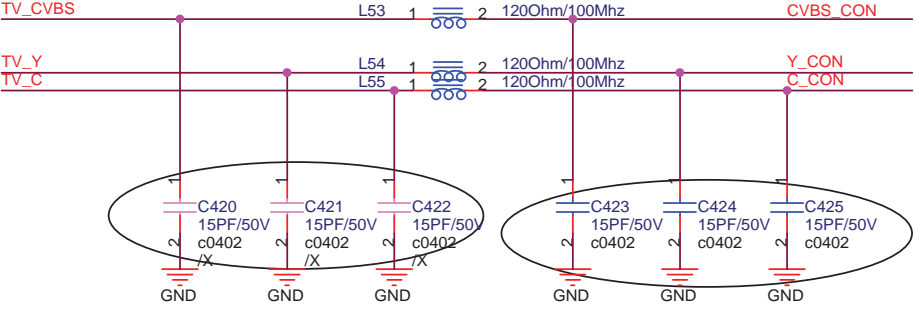




TV  
OUT

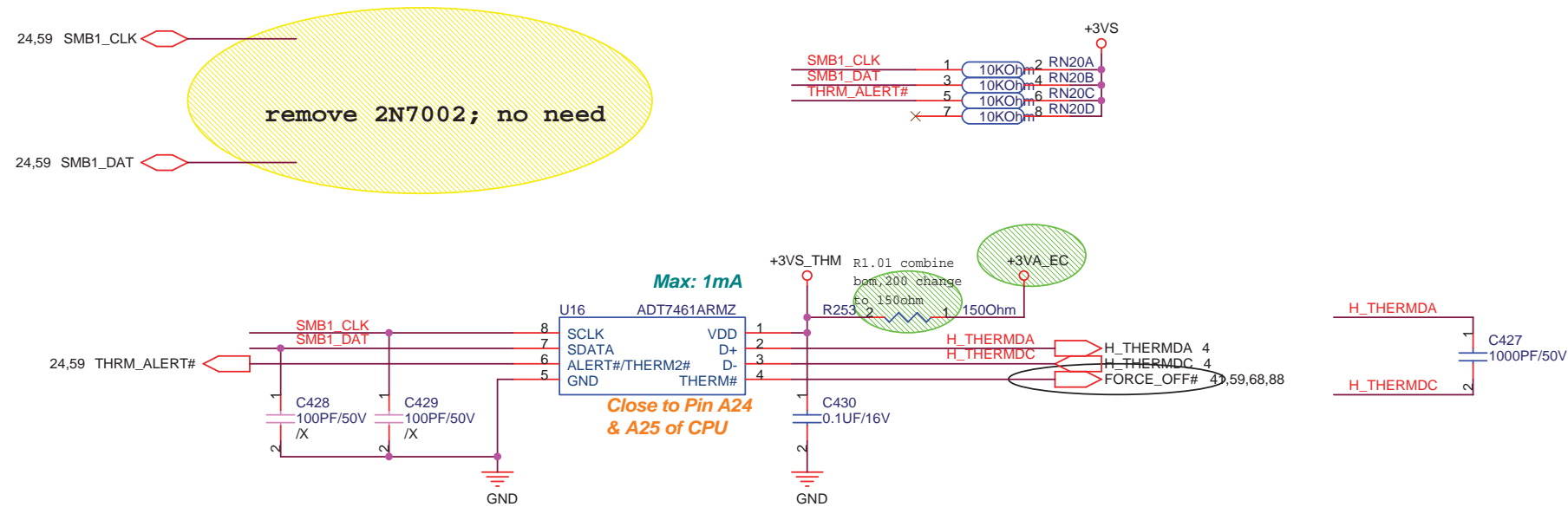


PLACE ESD  
Diodes near  
TV port



5	4	3	2	1
D				D
C				C
B				B
A				A
<div>ASUS ASUSTeK COMPUTER INC</div> <div><div>Size Custom</div><div>Project Name <b>Z96J</b></div><div>Rev 1.0</div></div> <div>Date: Wednesday, January 11, 2006Sheet 36 of 92</div>				
5	4	3	2	1

## Thermal Sensor



**Route H\_THERMDA and H\_THERMDC on the same layer**

## ---OTHER SIGNALS

**15 mils**



**GND**

**10 mils**

=====H\_THERMDA(10 mils)

**10 mils**

=====H\_THERMDC(10 mils)

**10 mils**

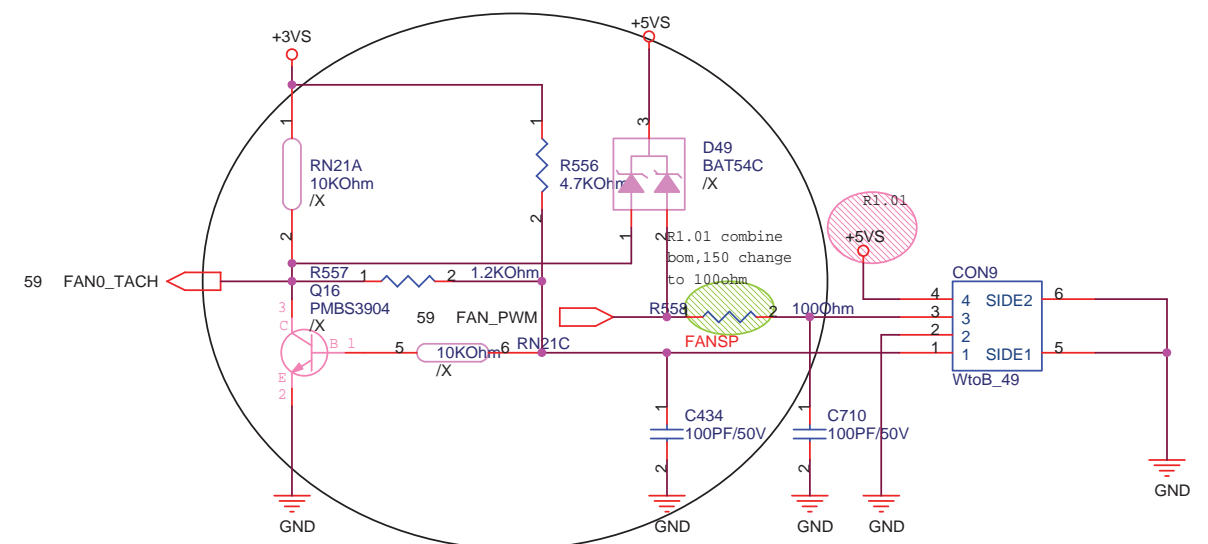
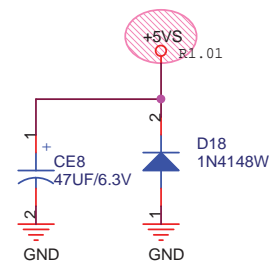
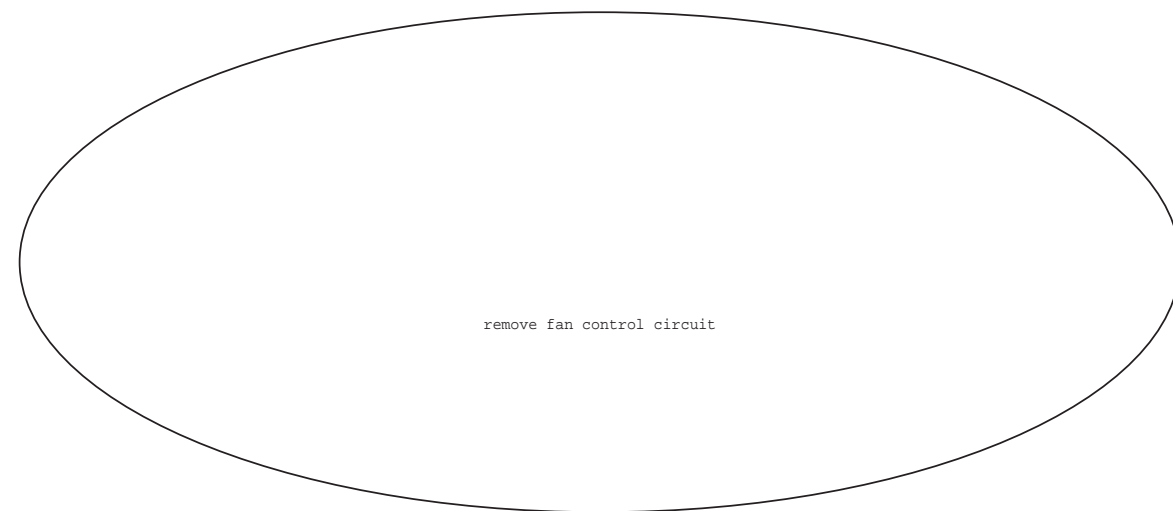


**15 mils**

## -----OTHER SIGNALS

**Avoid FSB,Power**

## DC FAN Control

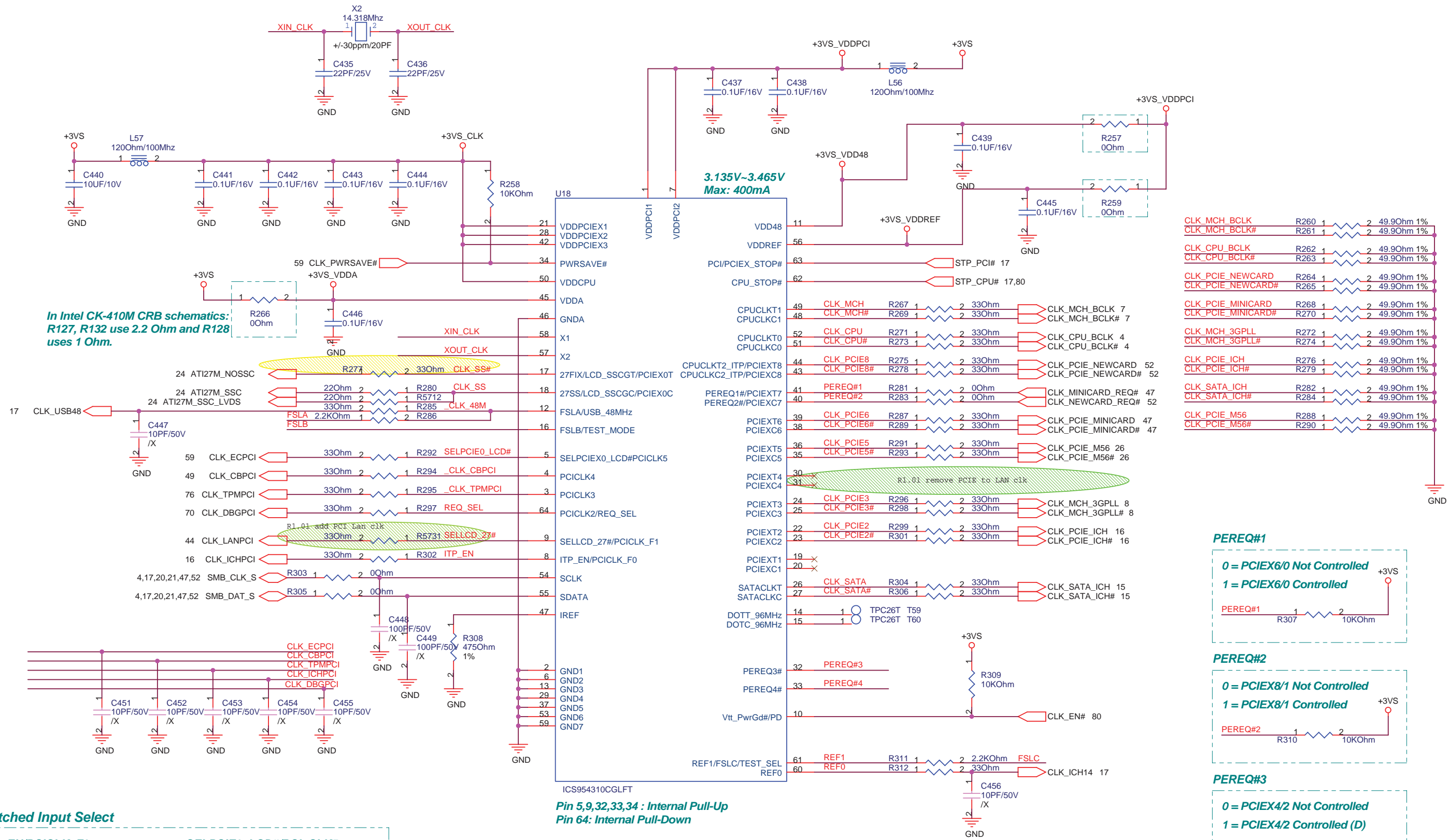


**CPU FAN will be forced on:**

- 1) Thermal Sensor Over-temperature
- 2) WATCHDOG asserted by EC

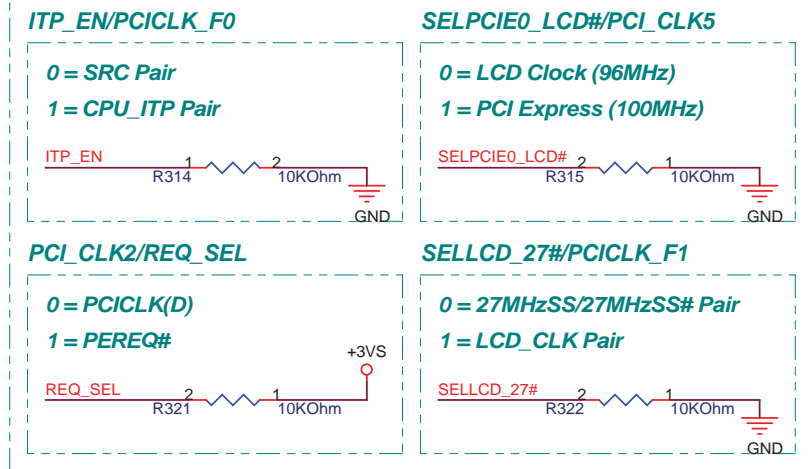






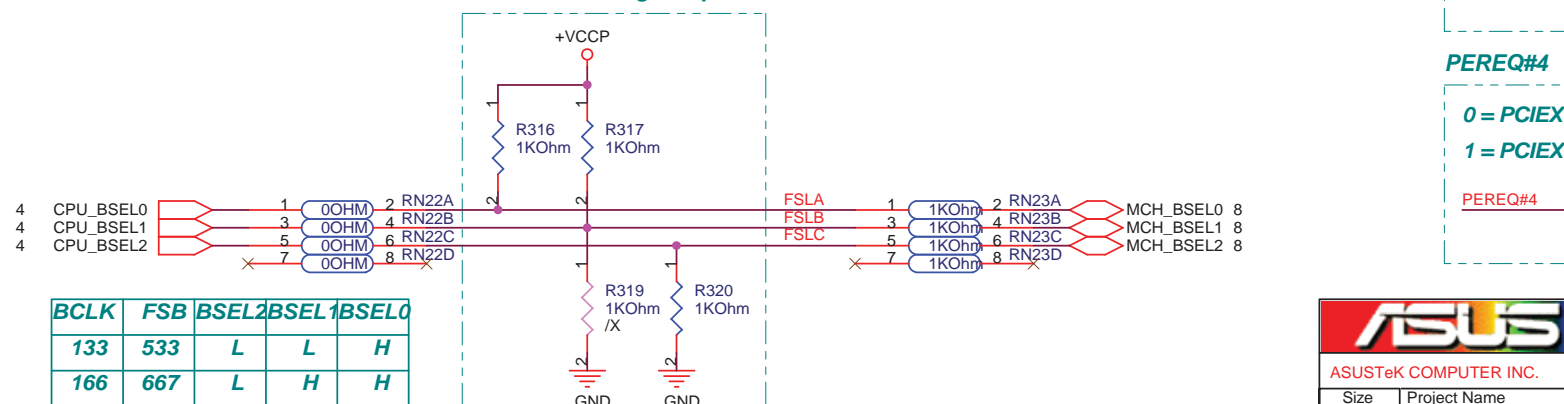
In Intel CK-410M CRB schematics:  
R127, R132 use 2.2 Ohm and R128  
uses 1 Ohm.

### Latched Input Select

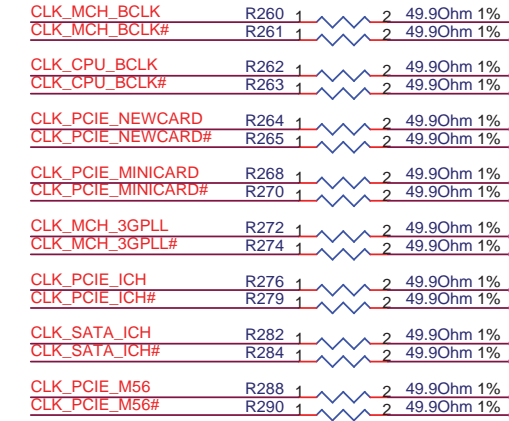


Pin 5,9,32,33,34 : Internal Pull-Up  
Pin 64: Internal Pull-Down

### Reserved for Debug & Expriment

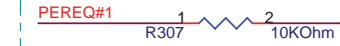


BCLK	FSB	BSEL	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



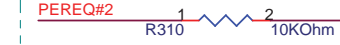
### PEREQ#1

0 = PCIEX6/0 Not Controlled  
1 = PCIEX6/0 Controlled



### PEREQ#2

0 = PCIEX8/1 Not Controlled  
1 = PCIEX8/1 Controlled



### PEREQ#3

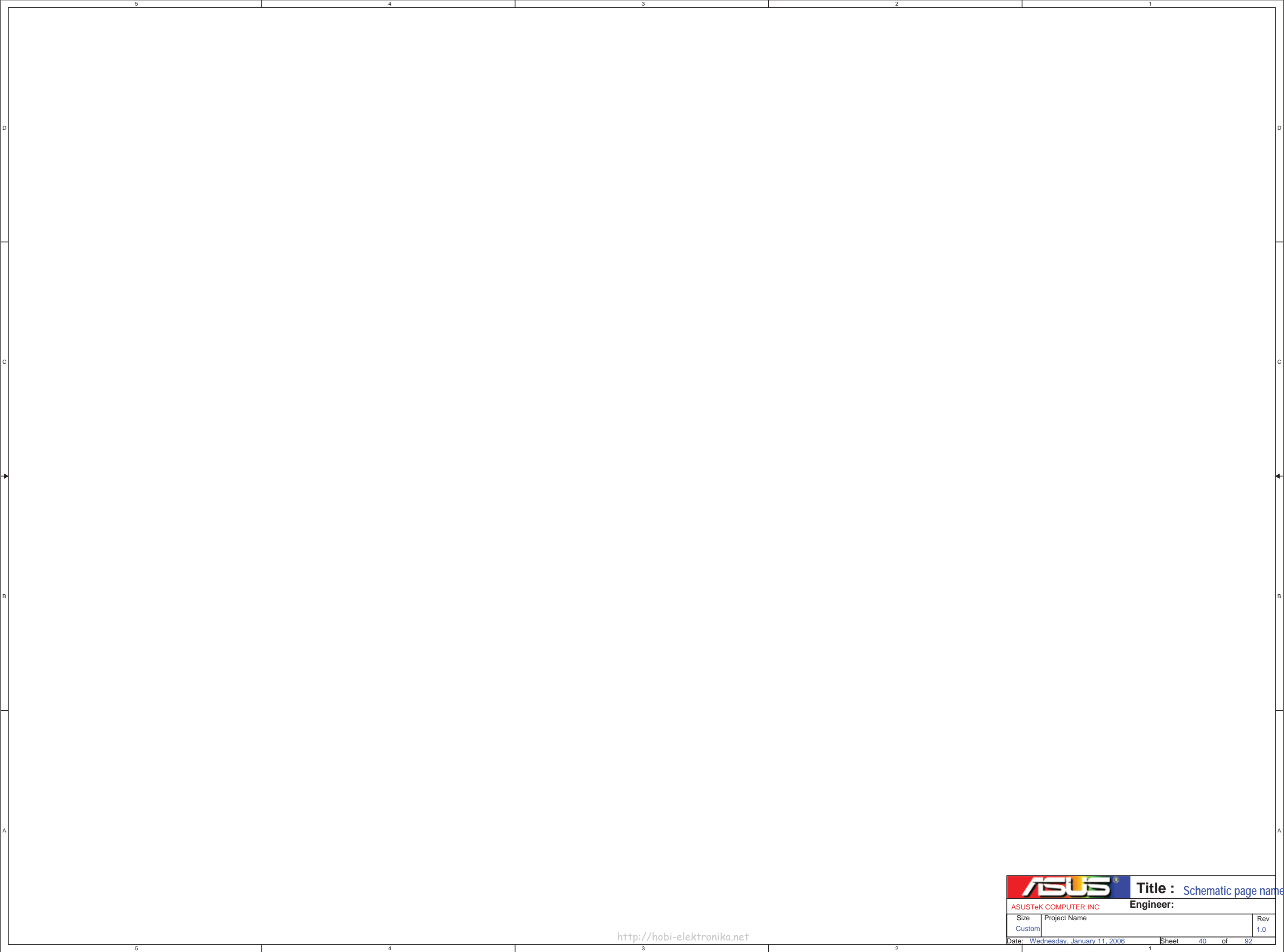
0 = PCIEX4/2 Not Controlled  
1 = PCIEX4/2 Controlled (D)




### PEREQ#4

0 = PCIEX7/5/3 Not Controlled  
1 = PCIEX7/5/3 Controlled (D)







**Title :** Schematic page name

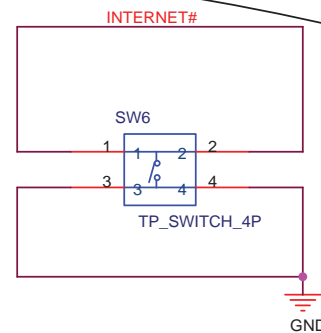
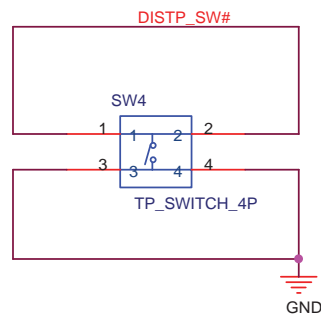
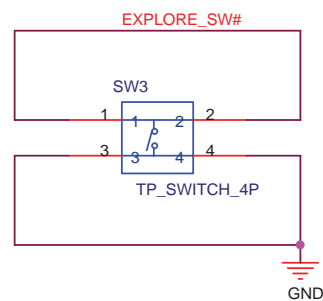
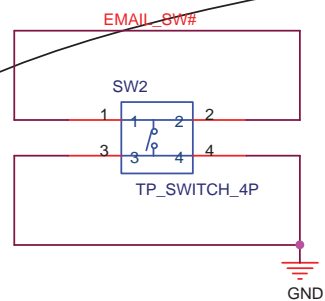
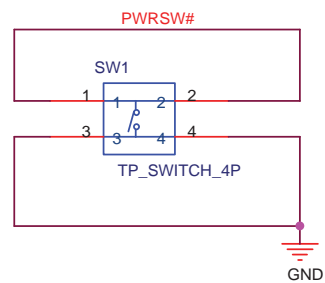
ASUSTeK COMPUTER INC

**Engineer:**

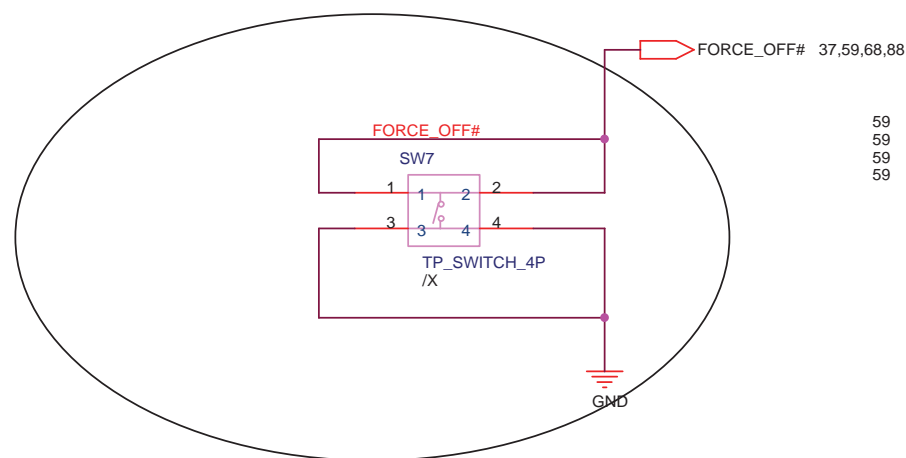
Size	Project Name	Rev
Custom		1.0

Date: Wednesday, January 11, 2006

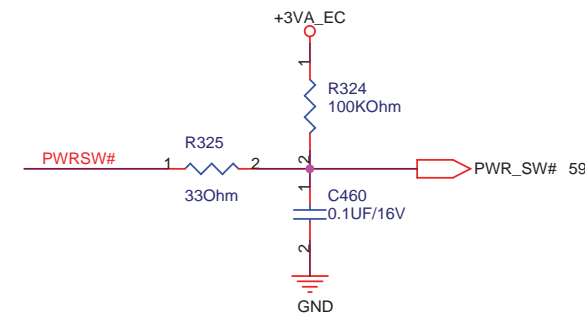
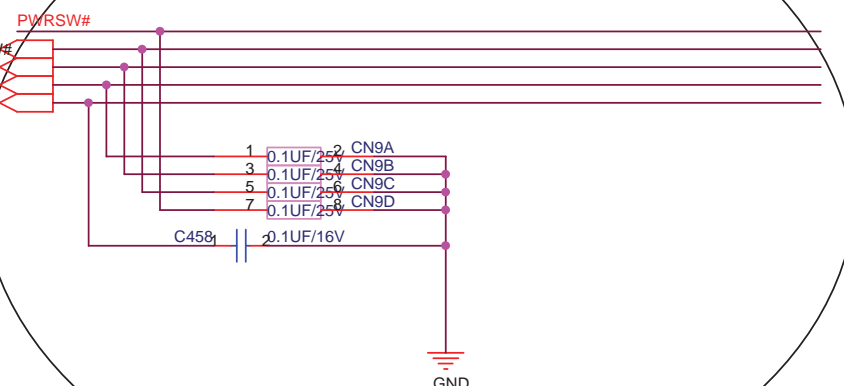
Sheet 40 of 92



## SHUT\_DOWN#



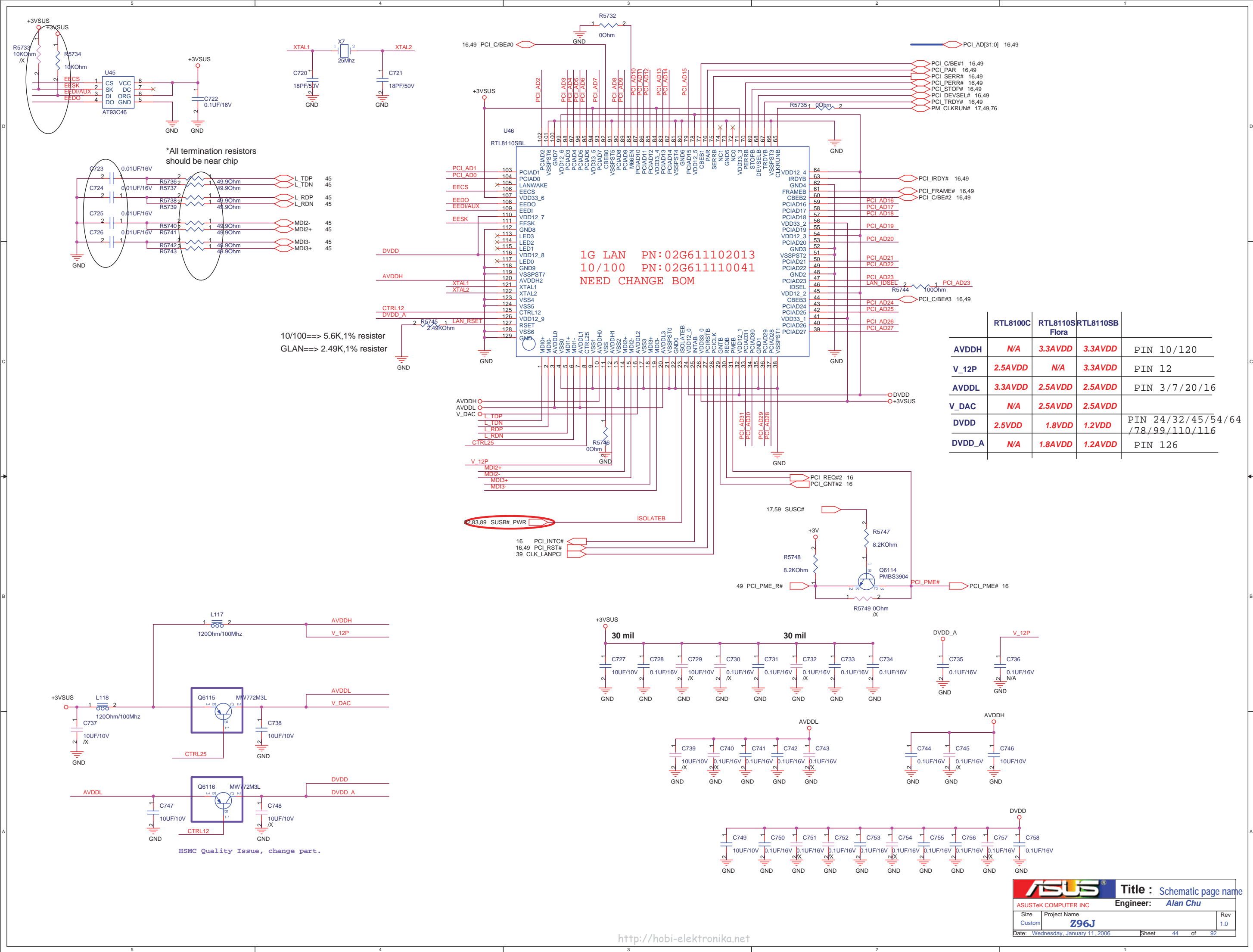
59 EXPLORE\_SW#  
59 DISTP\_SW#  
59 INTERNET#  
59 EMAIL\_SW#



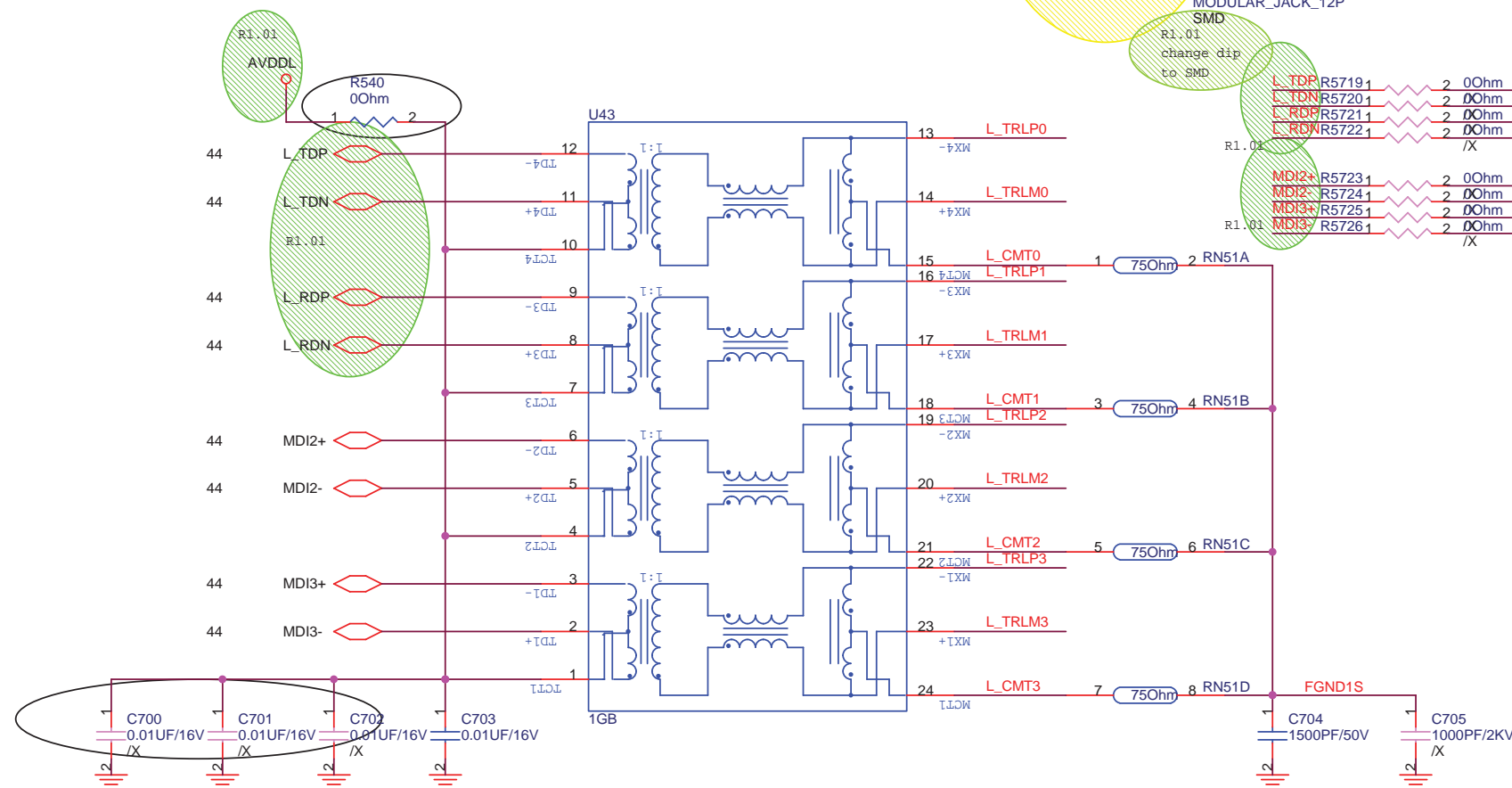
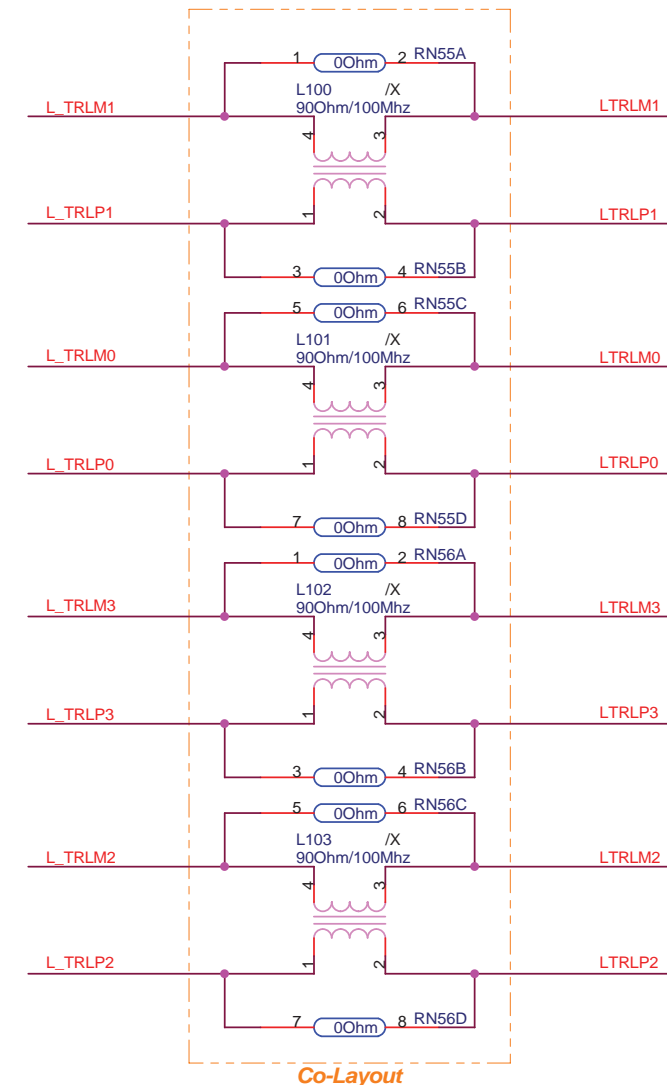
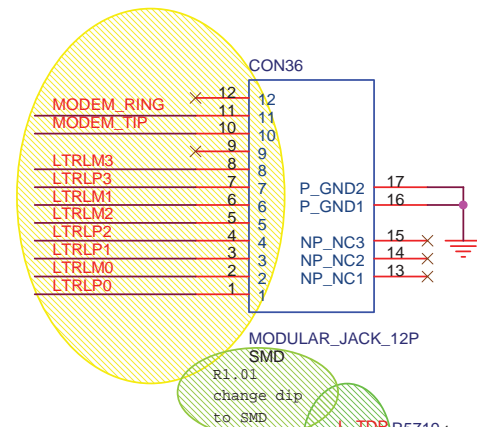
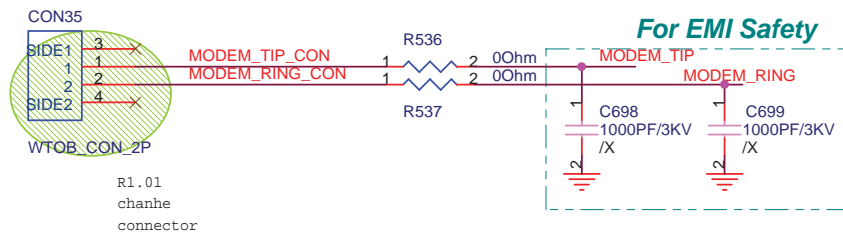
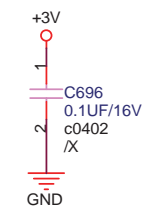
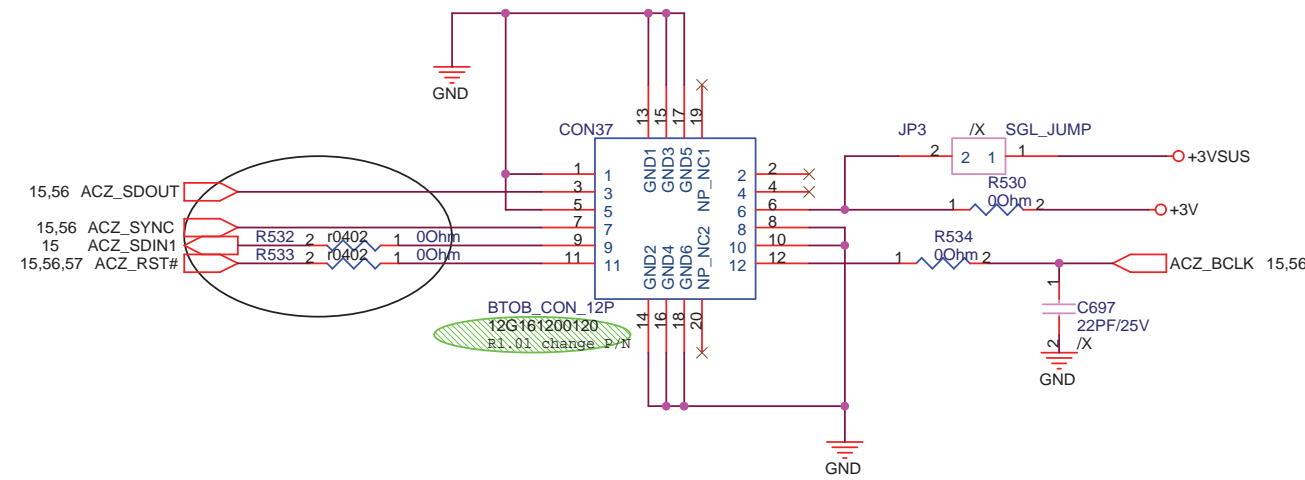


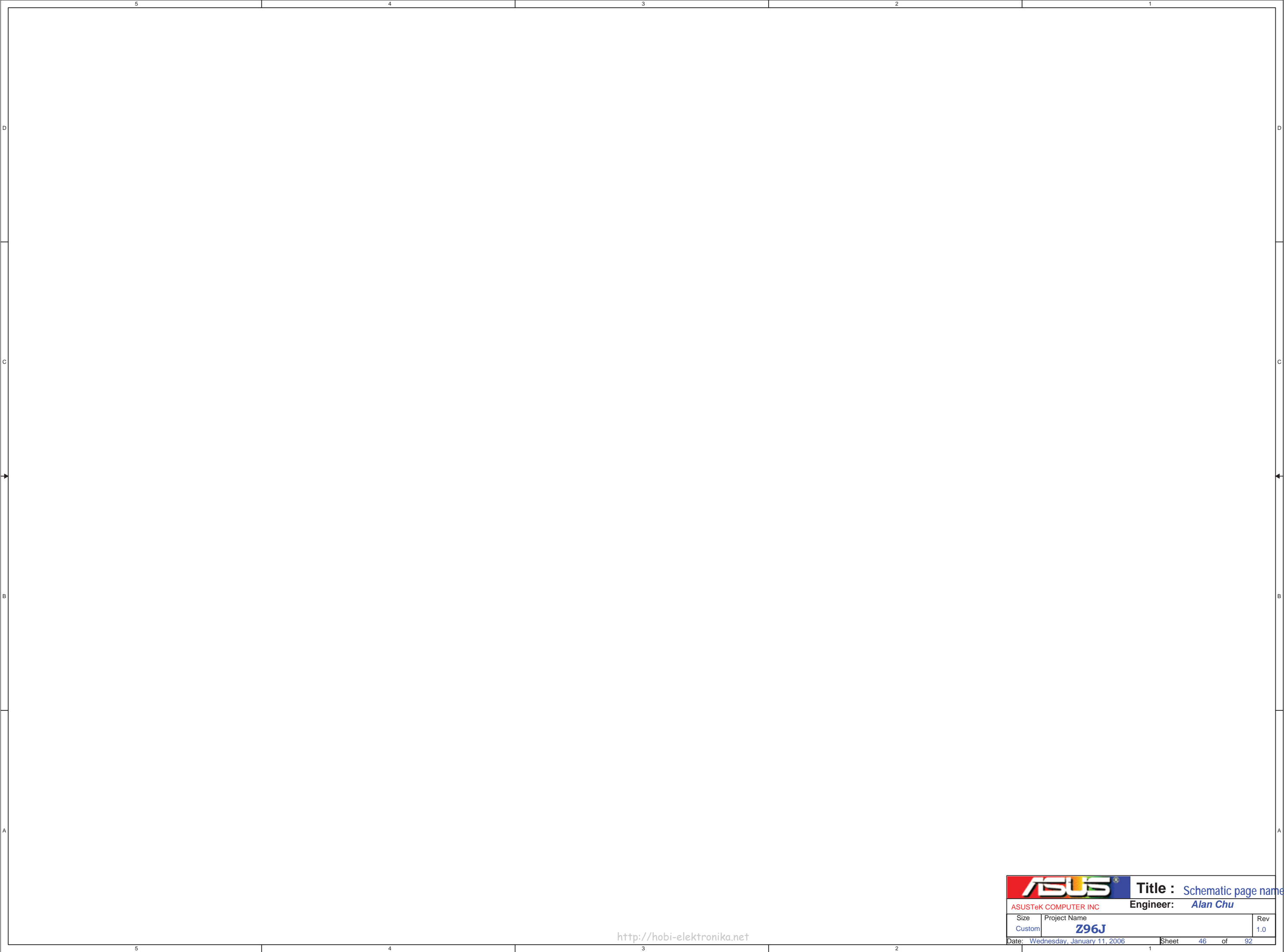
5	4	3	2	1
D				D
C				C
B				B
A				A
<div>ASUS®</div> <div>ASUSTeK COMPUTER INC</div> <div>Size: CustomProject Name: Z96J</div> <div>Date: Wednesday, January 11, 2006</div>				
Title : Schematic page name				Engineer: Alan Chu
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# MDC CONN.

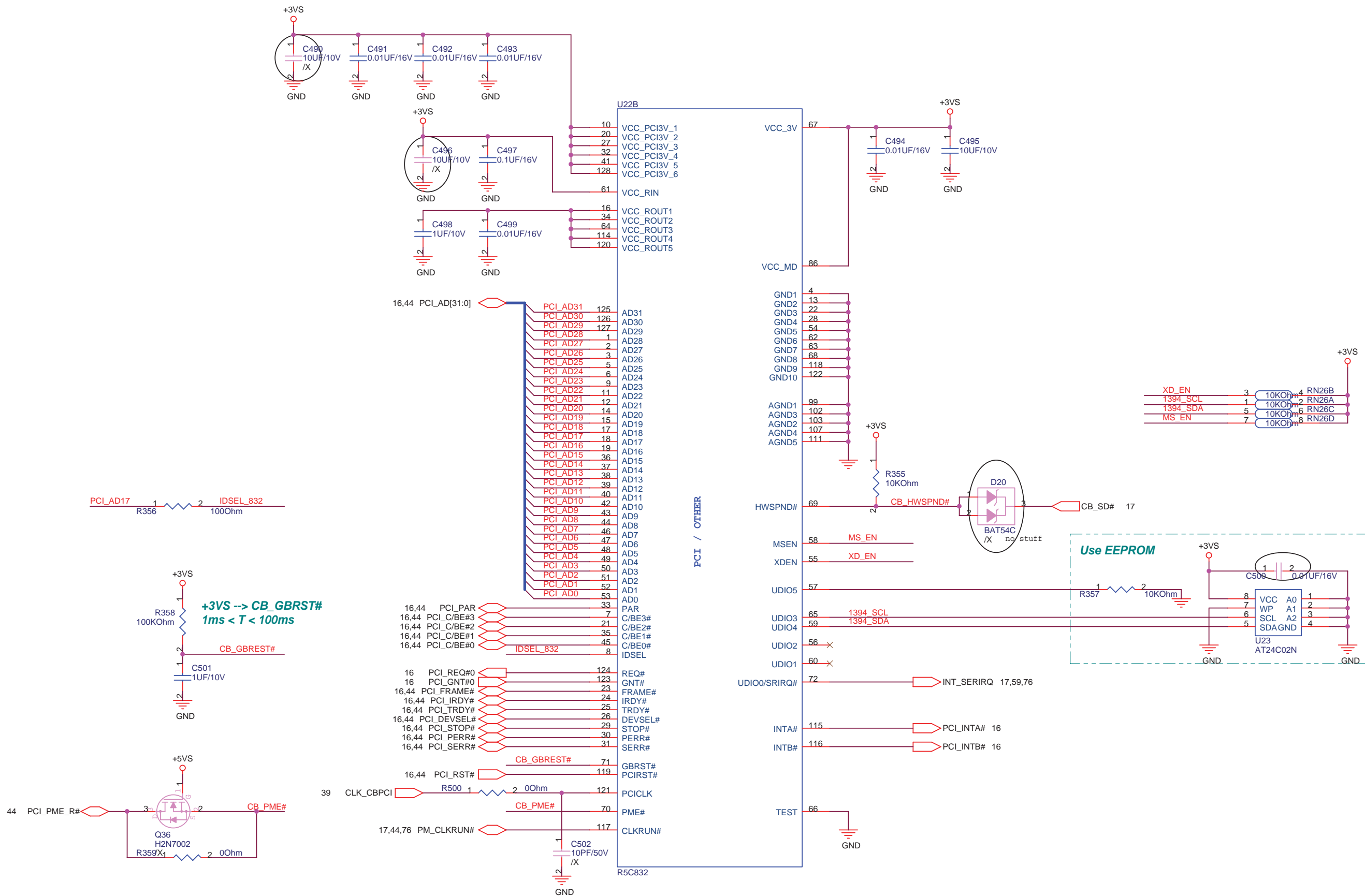






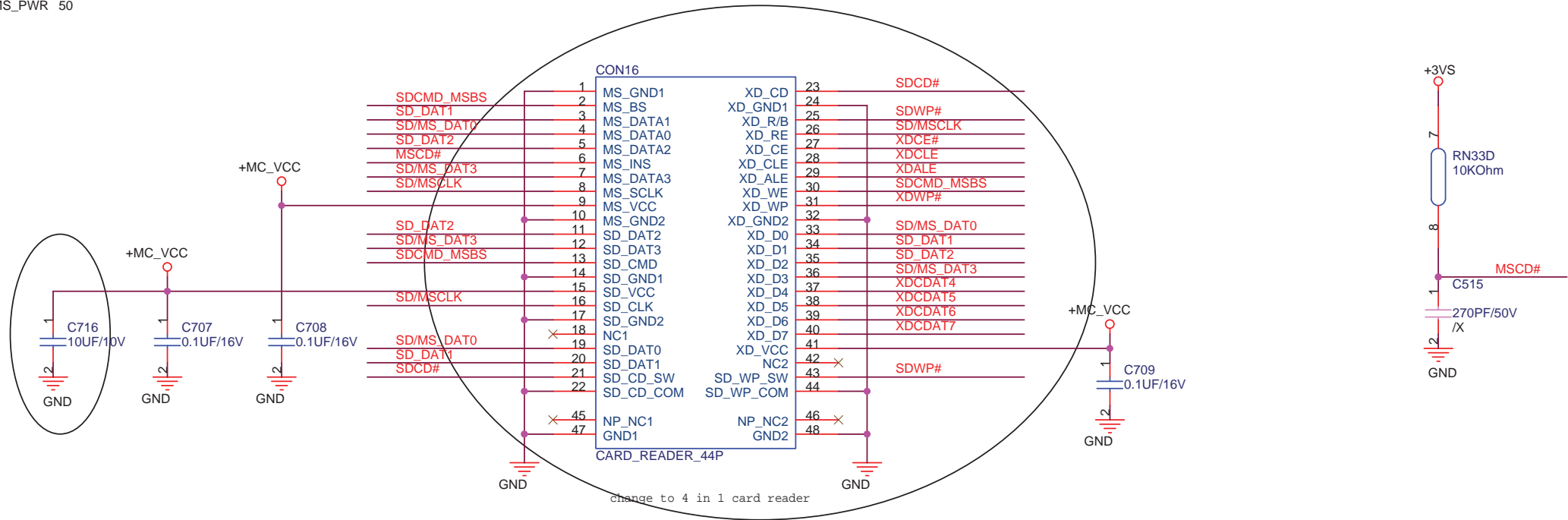
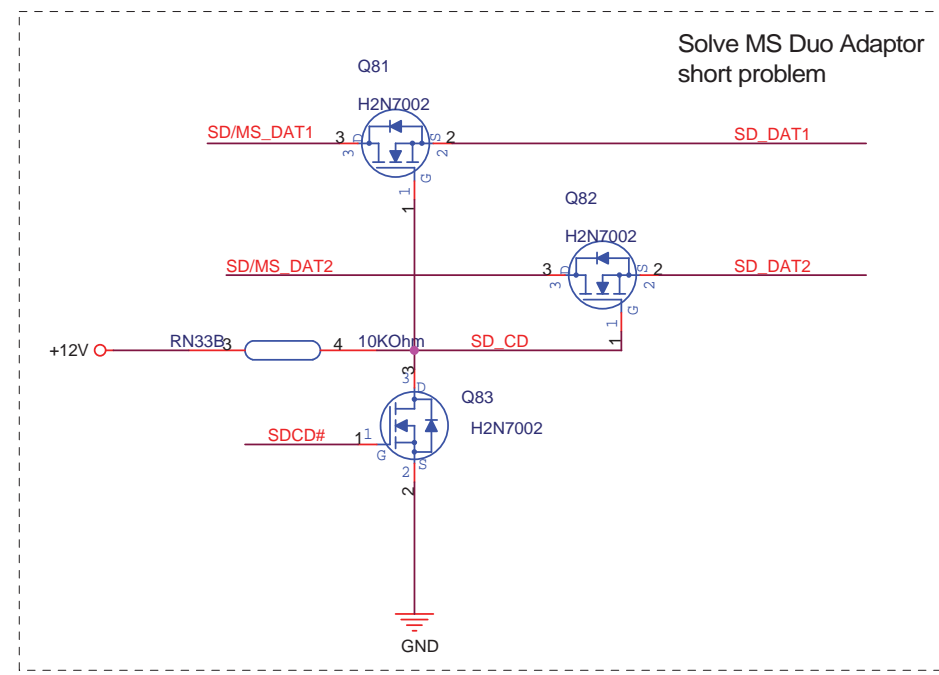
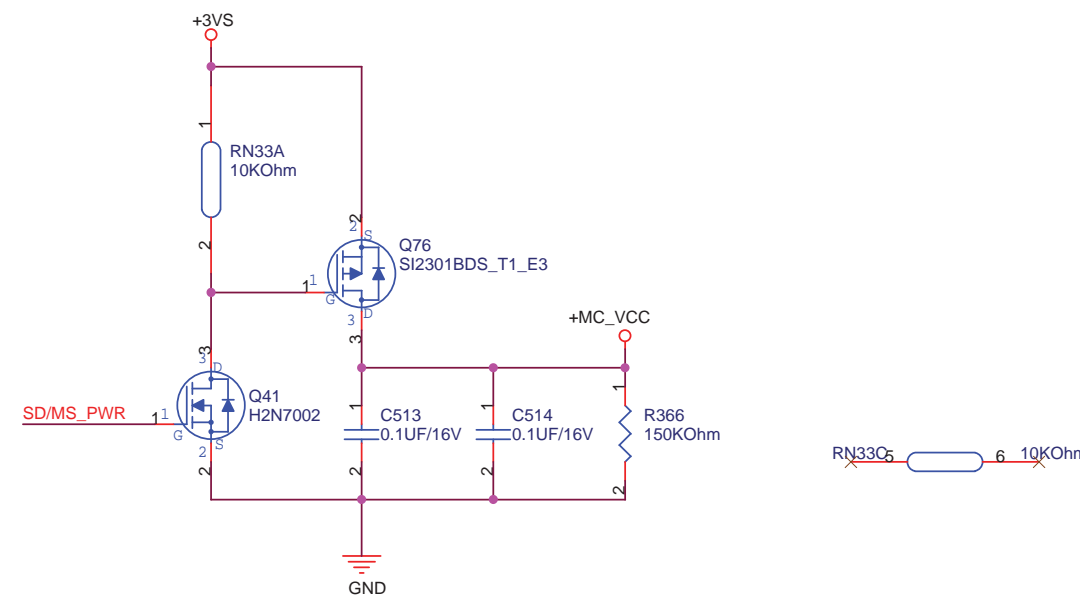


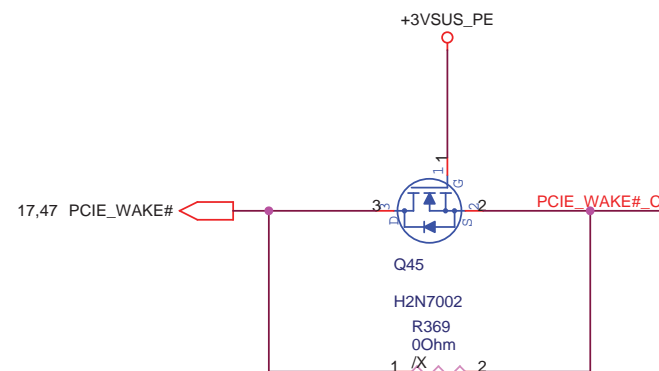
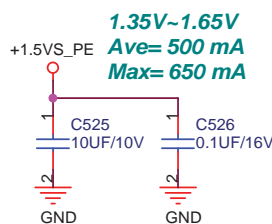
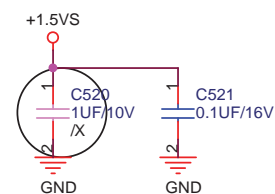
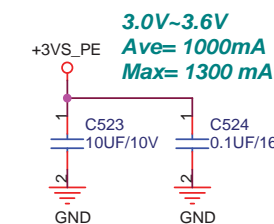
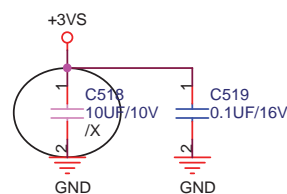
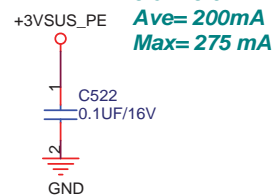
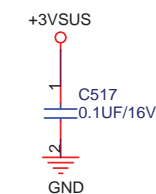
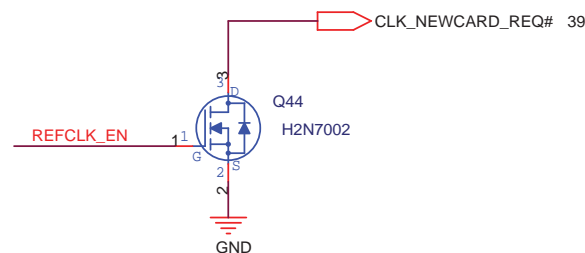
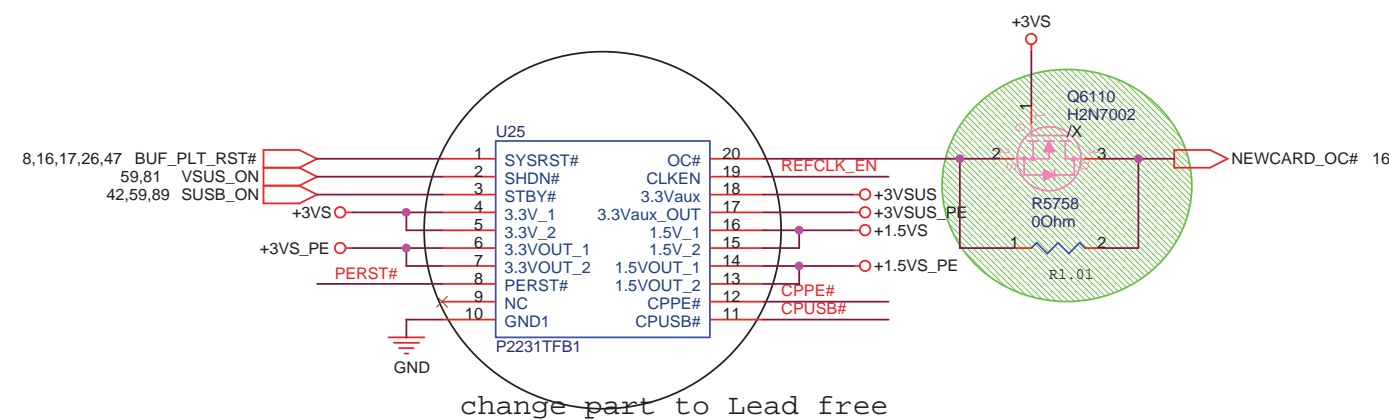
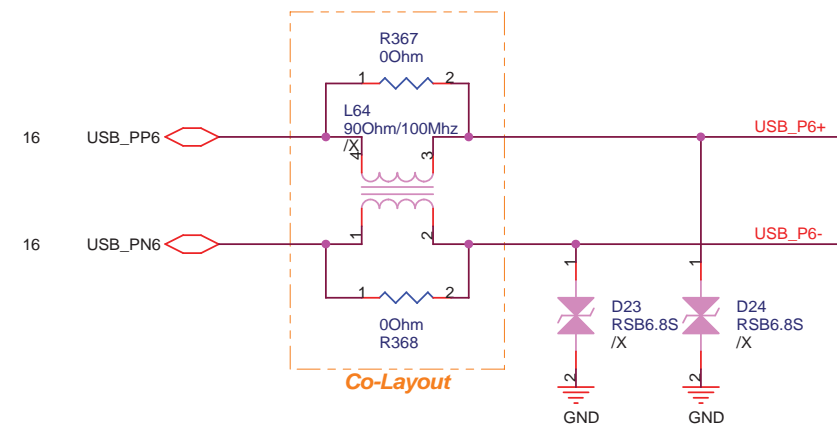




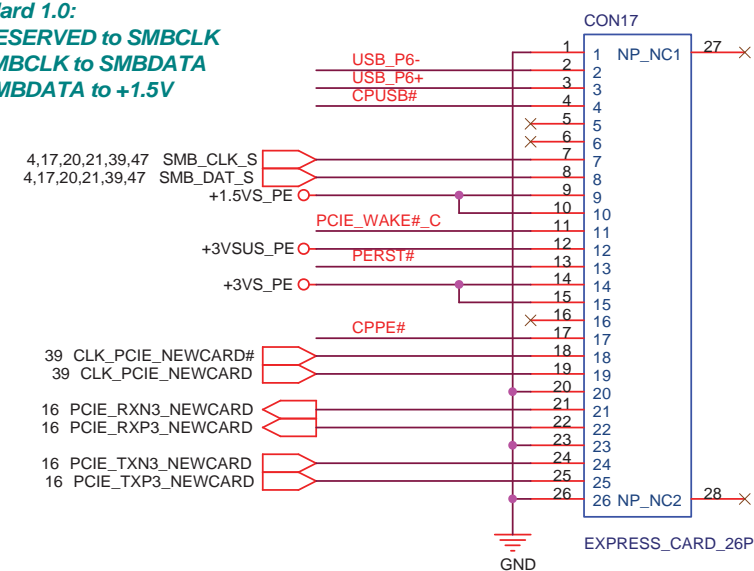


- XDCDAT7 50
- XDCDAT6 50
- XDCDAT5 50
- XDCDAT4 50
- SD/MS\_DAT3 50
- SD/MS\_DAT2 50
- SD/MS\_DAT1 50
- SD/MS\_DAT0 50
- XDWP# 50
- SDCMD\_MSBS 50
- XDALE 50
- XDCLE 50
- XDCE# 50
- SDWP# 50
- SDCD# 50
- MSCD# 50
- SD/MSCLK 50
- SD/MS\_PWR 50



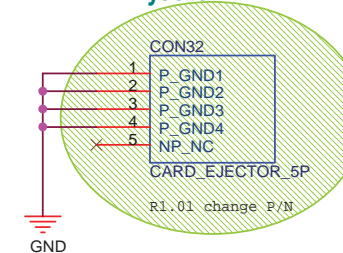


!! ExpressCard Standard 1.0:  
Change Pin7 from RESERVED to SMBCLK  
Change Pin8 from SMBCLK to SMBDATA  
Change Pin9 from SMBDATA to +1.5V



## NewCard Header

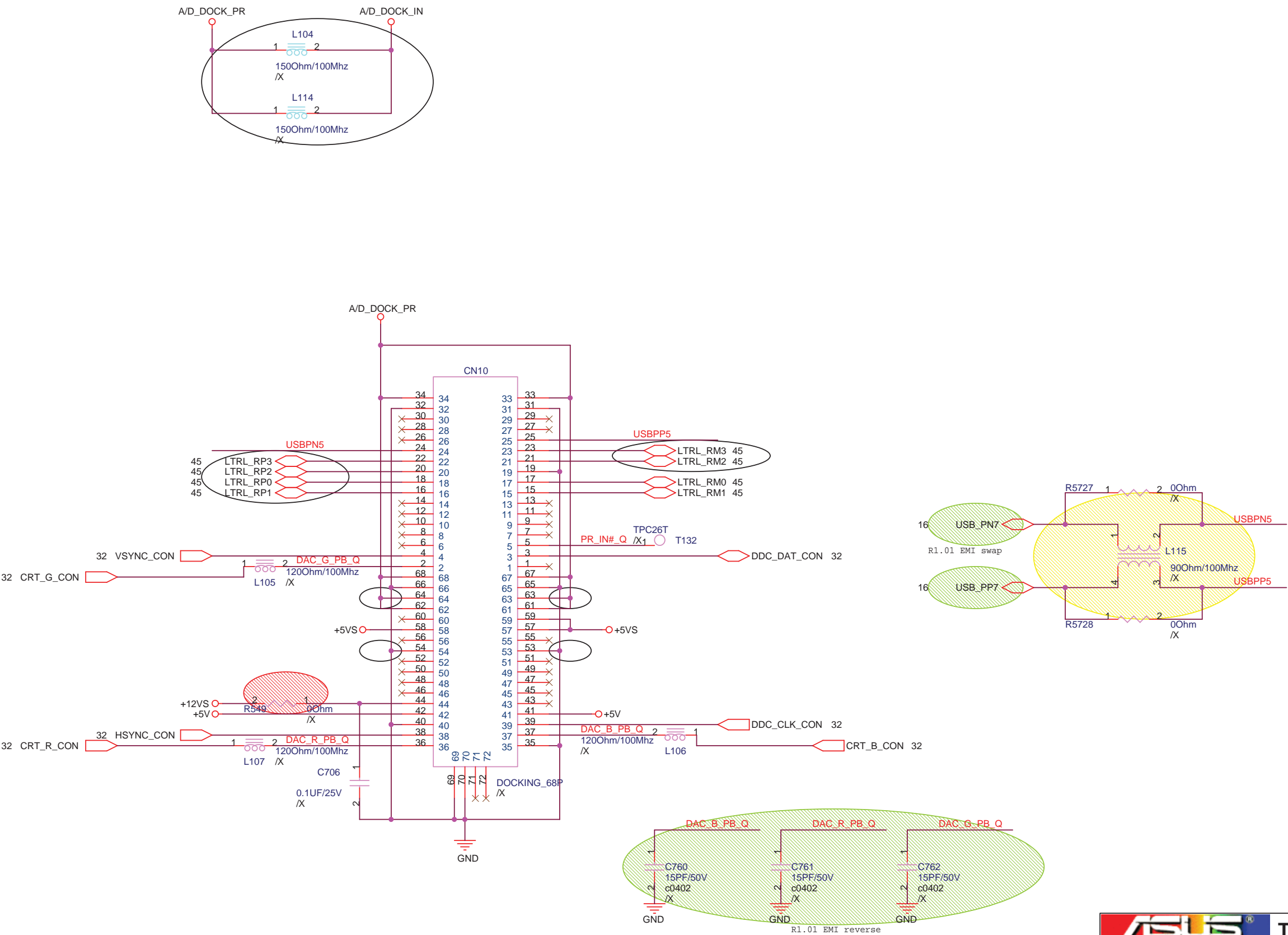
## NewCard Ejecter



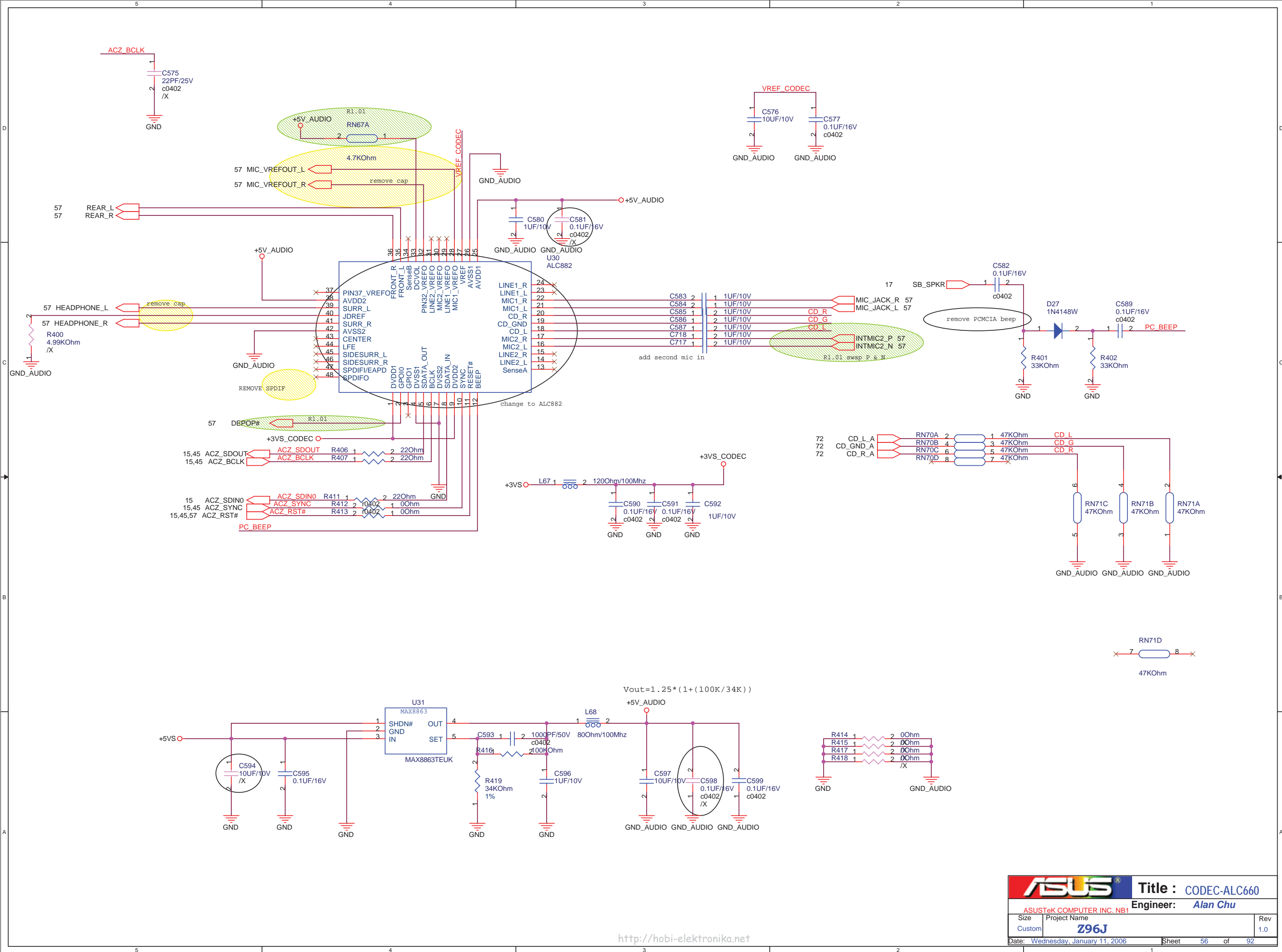


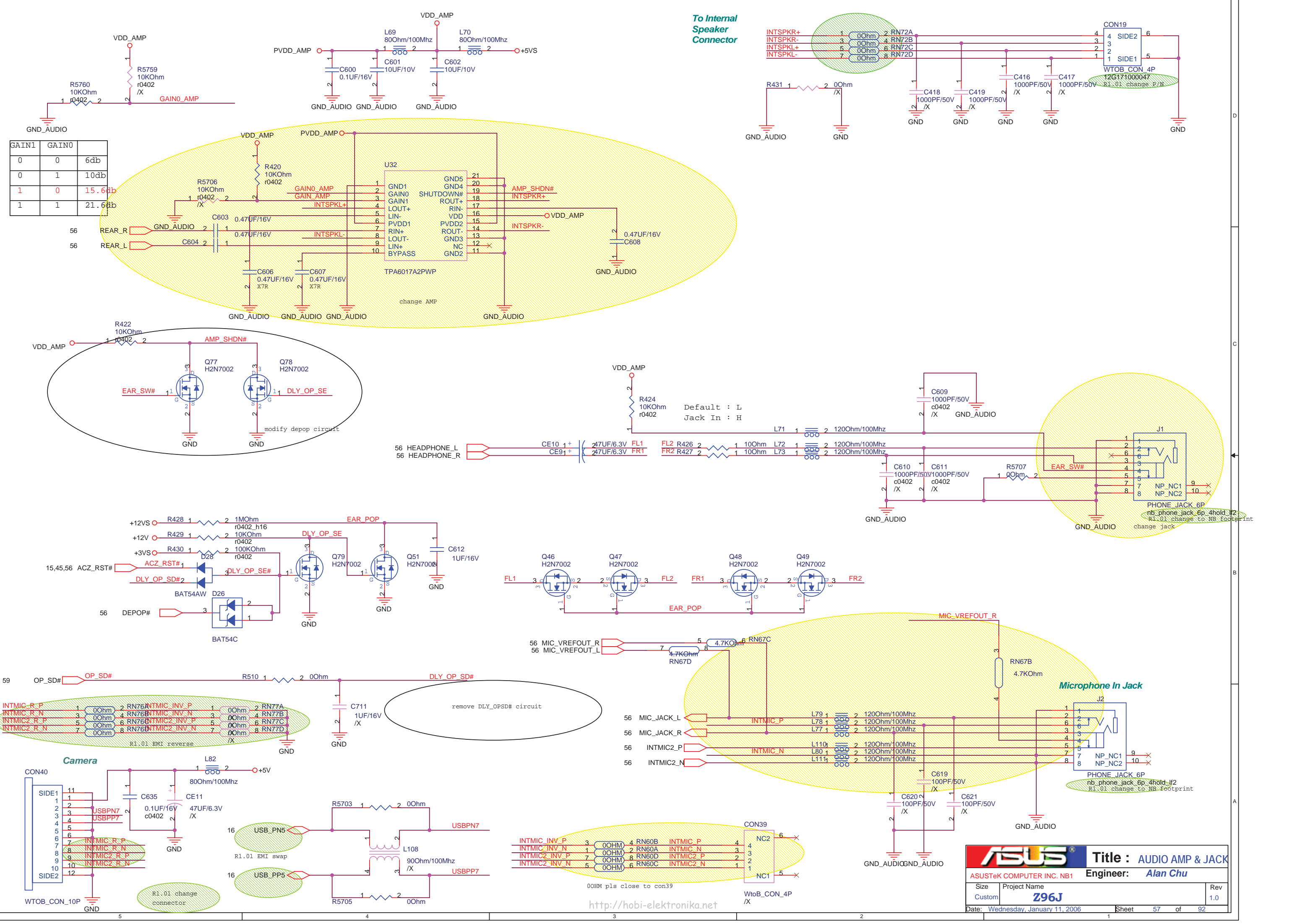
5					4					3					2					1				
D																								
C																								
B																								
A																								
																				</				

PORT BAR III









GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



Title : AUDIO AMP & JACK

ASUSTek COMPUTER INC. NB1

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96J	1.0

Date: Wednesday, January 11, 2006Sheet 57 of 92

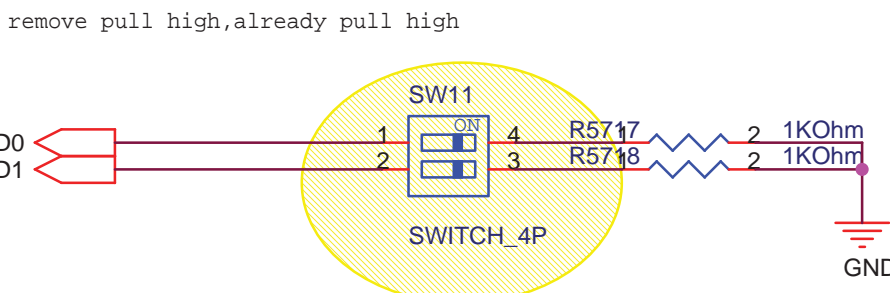
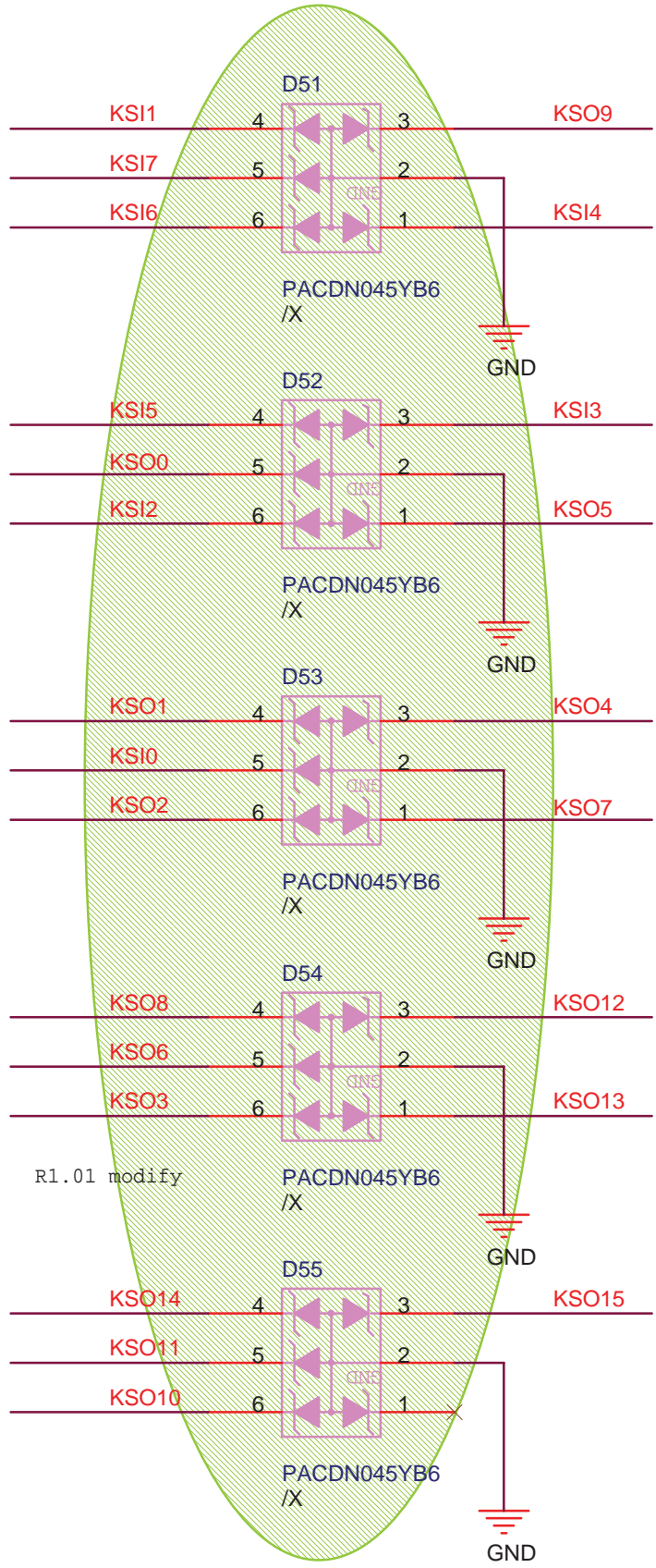
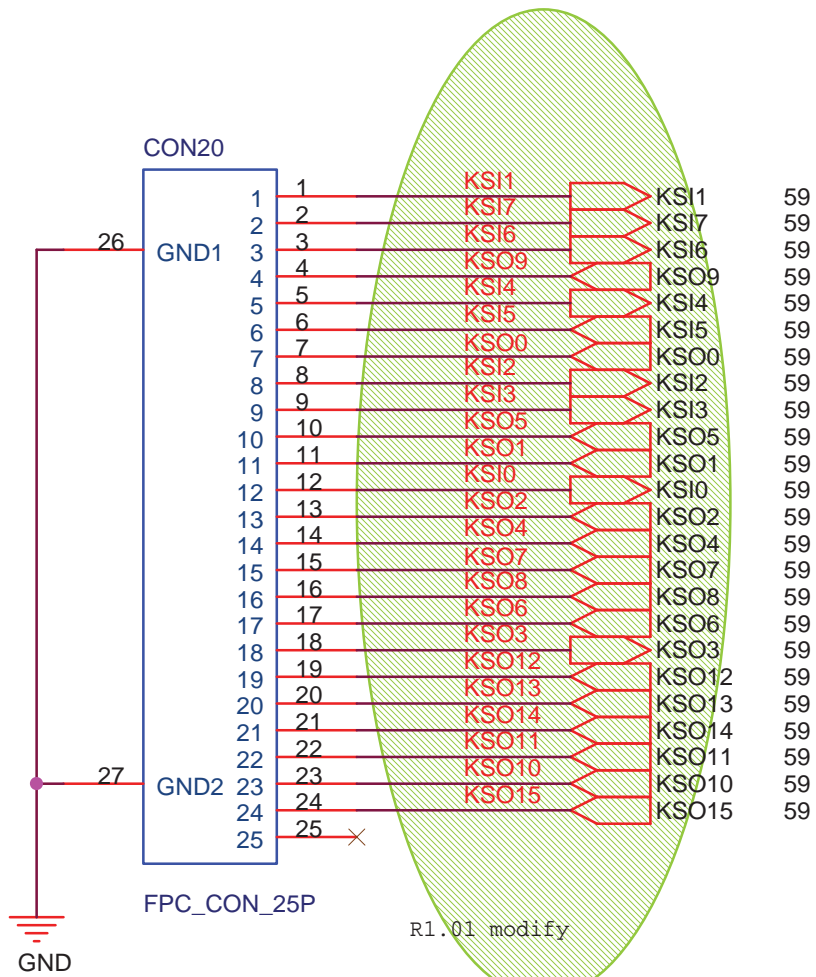
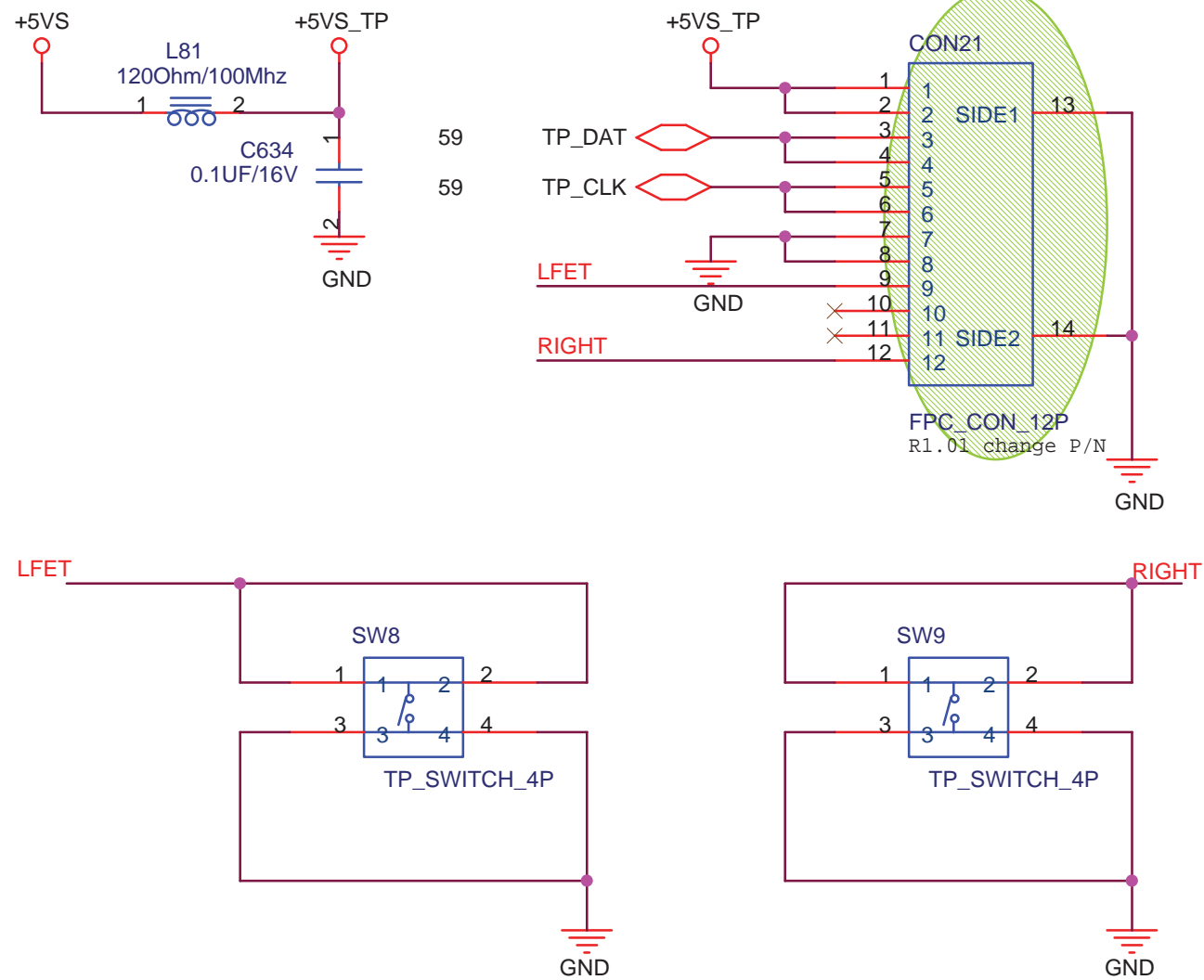


5	4	3	2	1
D				D
C				C
B				B
A				A
<div>ASUS®</div> <div>ASUSTeK COMPUTER INC</div> <div>Size: CustomProject Name: Z96J</div> <div>Date: Wednesday, January 11, 2006</div>				
Title : Schematic page name				Engineer: Alan Chu
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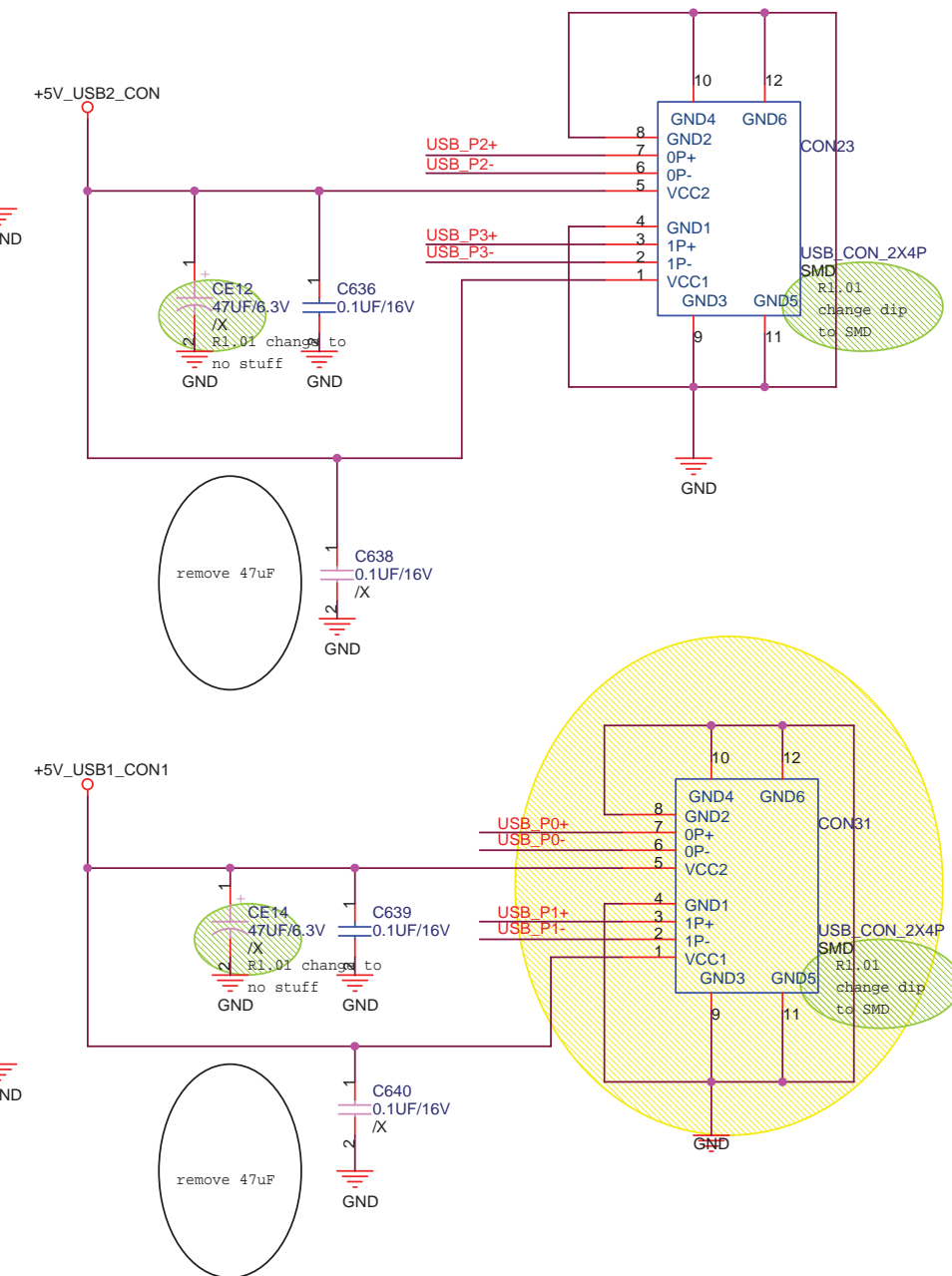
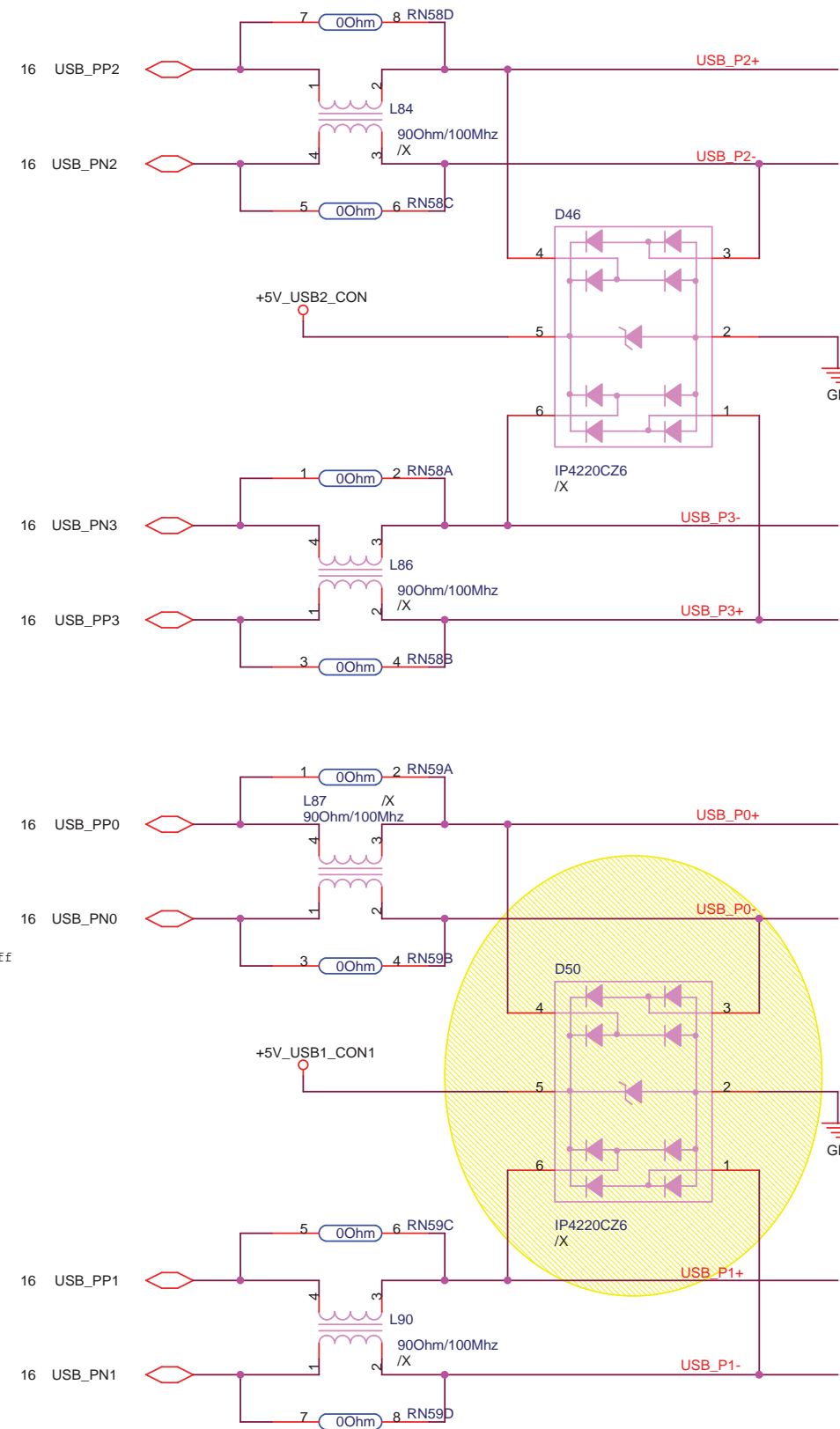
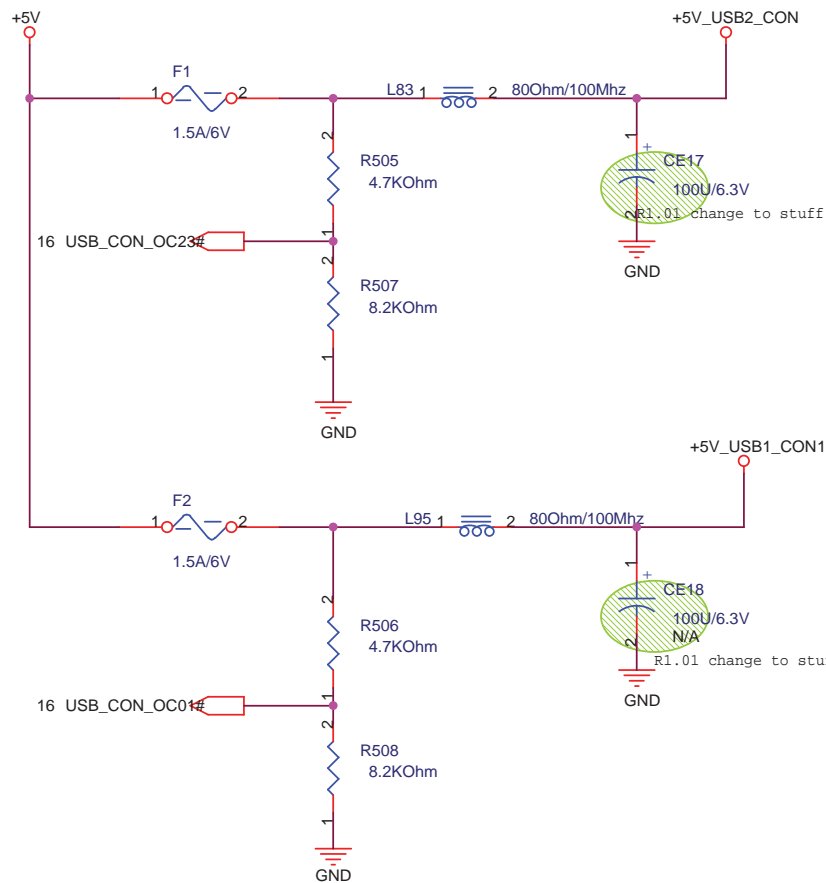


For Touch-Pad

For Keyboard









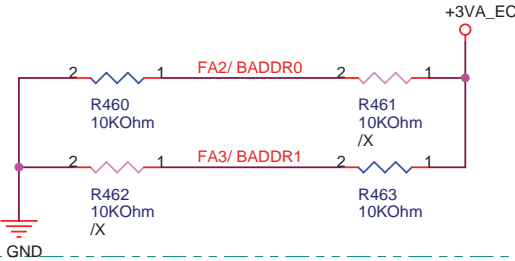


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

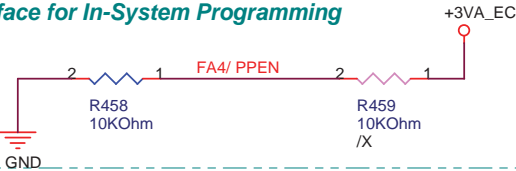
00: PNPCNG Access Register Pair Are 002Eh and 002Fh  
10: PNPCNG Access Register Pair Are 004Eh and 004Fh  
01: PNPCNG Access Register Pair Are Determined by  
EC Domain Registers SWCBALR and SWCBAHR.  
11: Reserved



Note: Sampled at VSTBY Power Up Reset

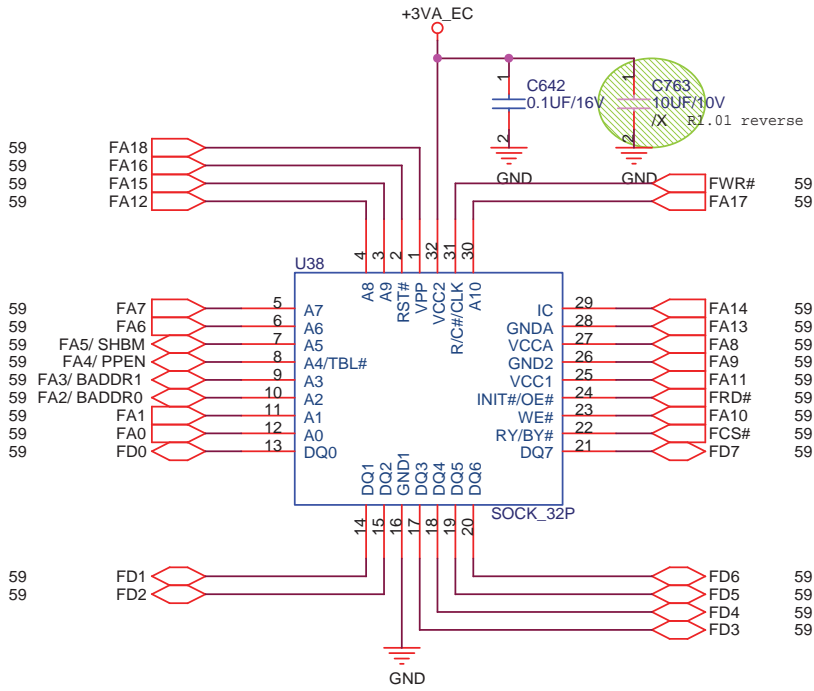
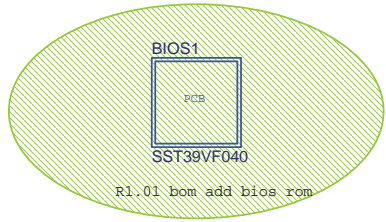
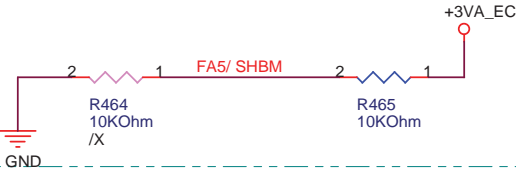
FA4/ PPEN

0: Normal  
1: KBS Interface Pins Are Switched to Parallel Port  
Interface for In-System Programming



FA5/ SHBM

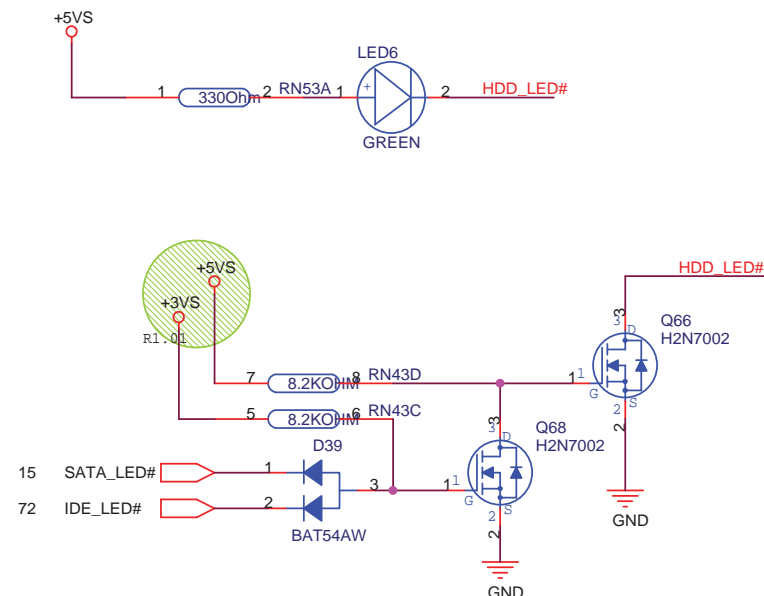
0: Disable Shared Memory with Host BIOS  
1: Enable Shared Memory with Host BIOS



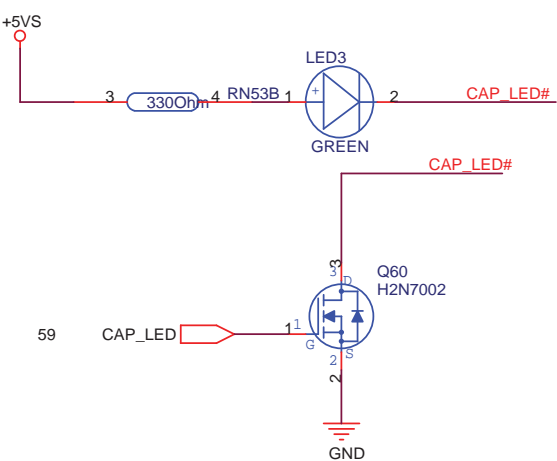


# For LED

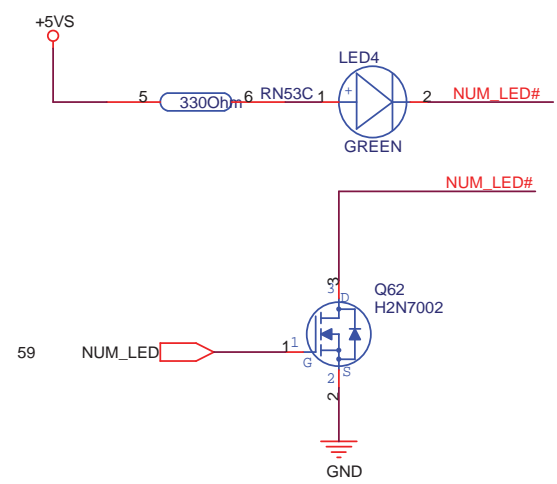
## For SATA/IDE LED



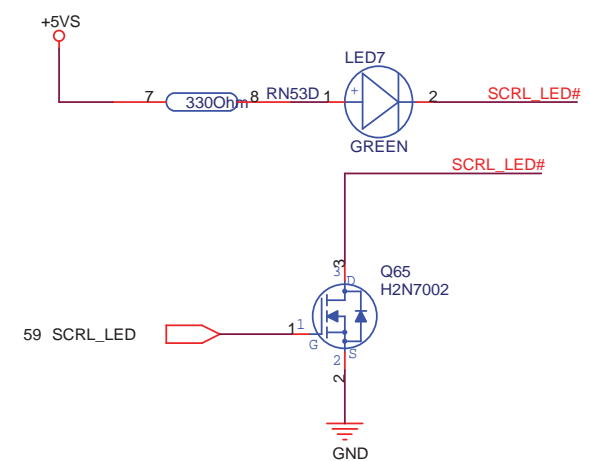
## for Cap. Lock



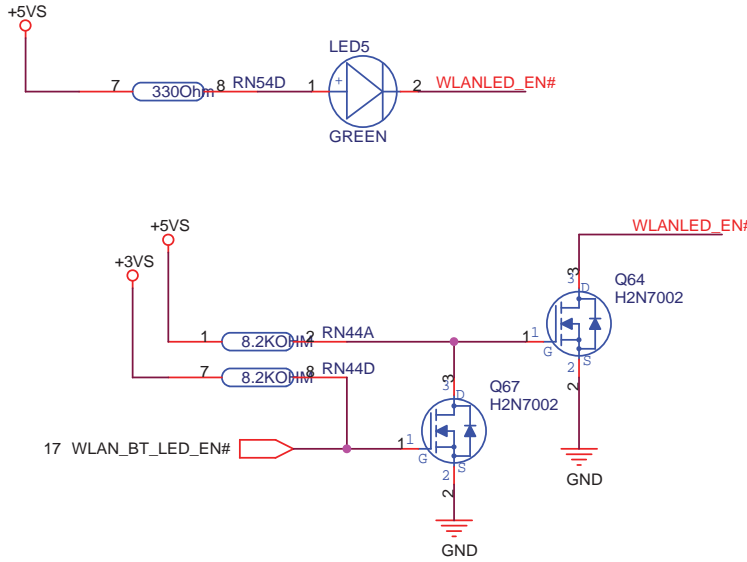
## for Num Lock



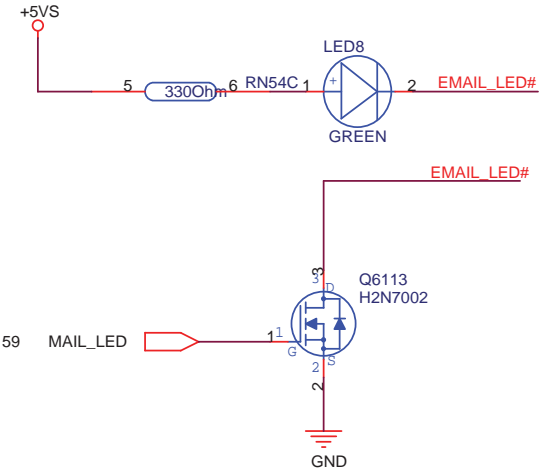
## for Scroll Lock



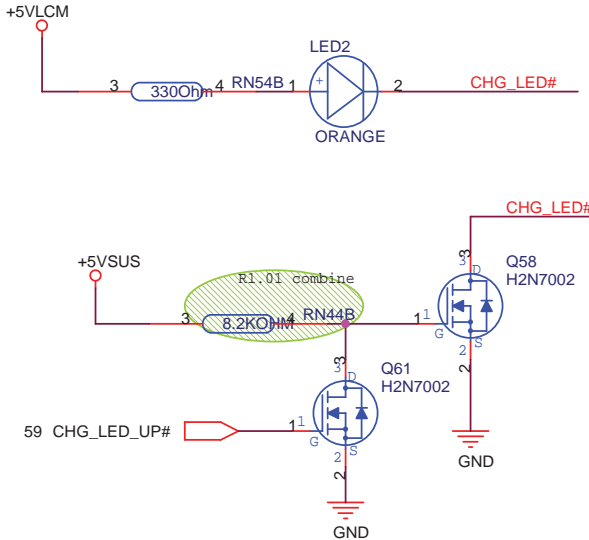
## For WireLess LED



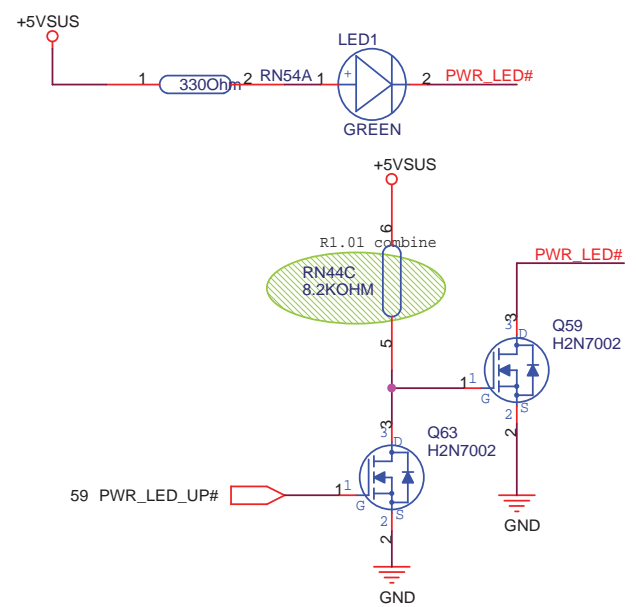
## for email

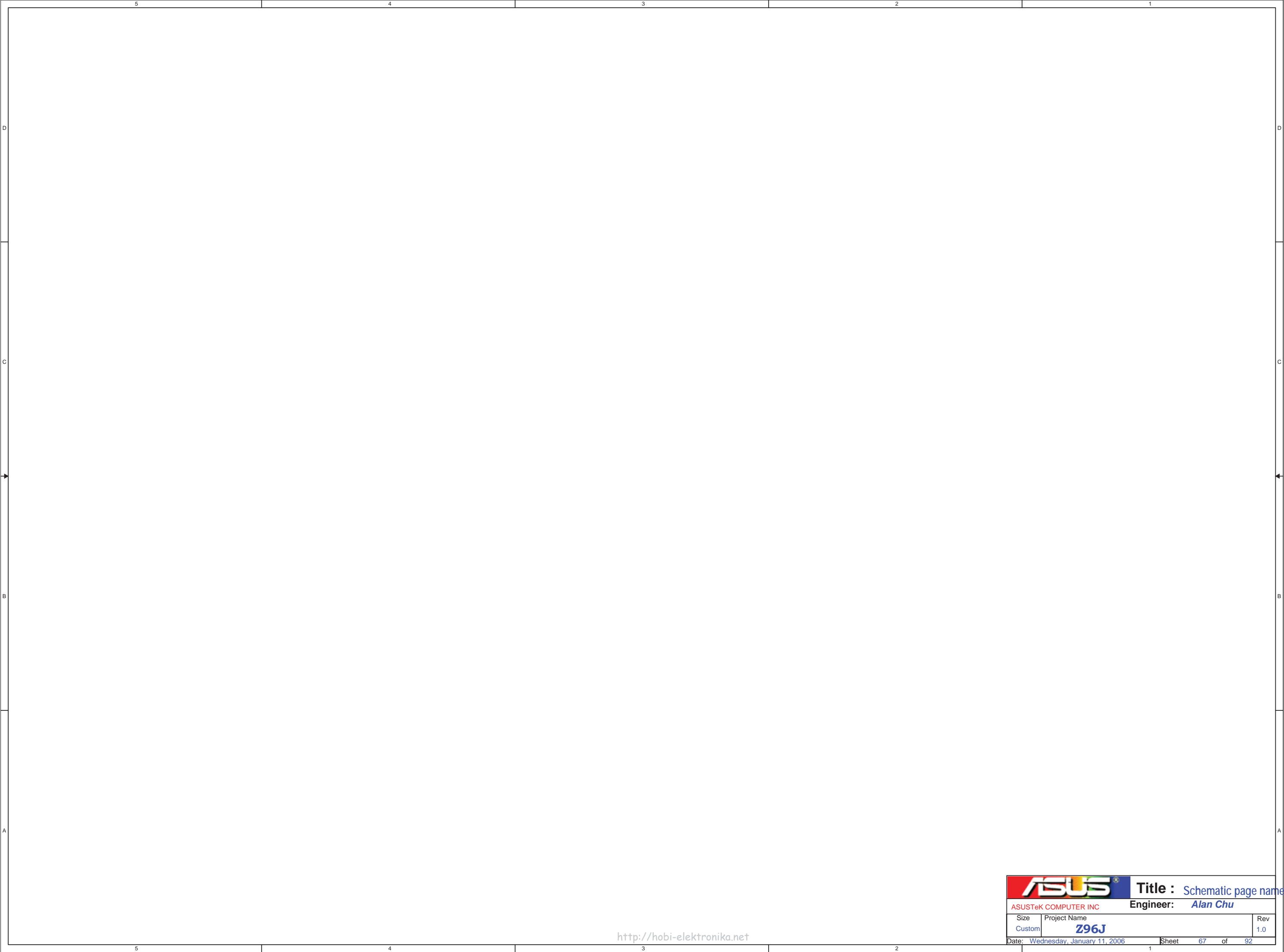



## For BATTERY LED



## For POWER LED







**Title :** Schematic page name

ASUSTeK COMPUTER INC

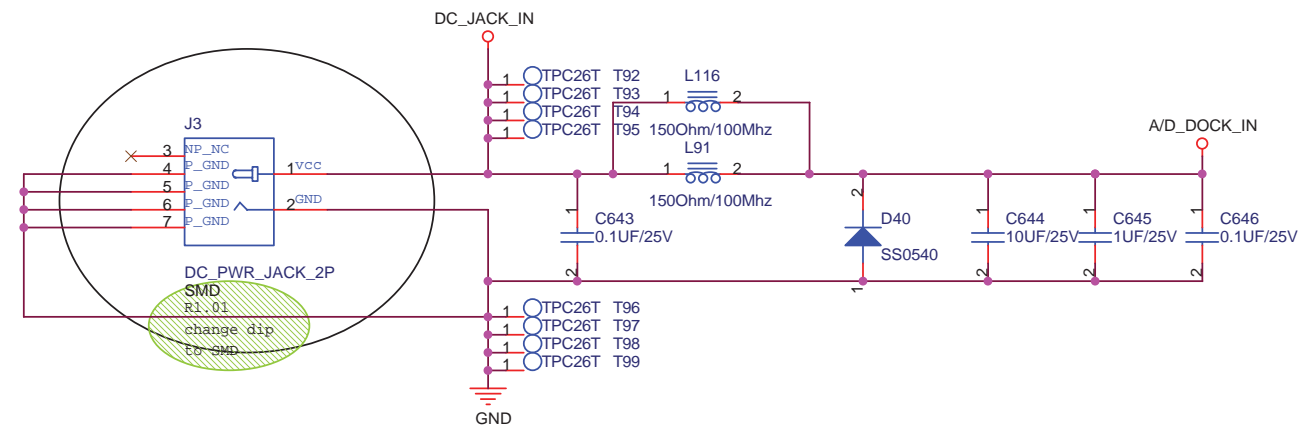
**Engineer:** Alan Chu

Size	Project Name	Rev
Custom	Z96J	1.0

Date: Wednesday, January 11, 2006

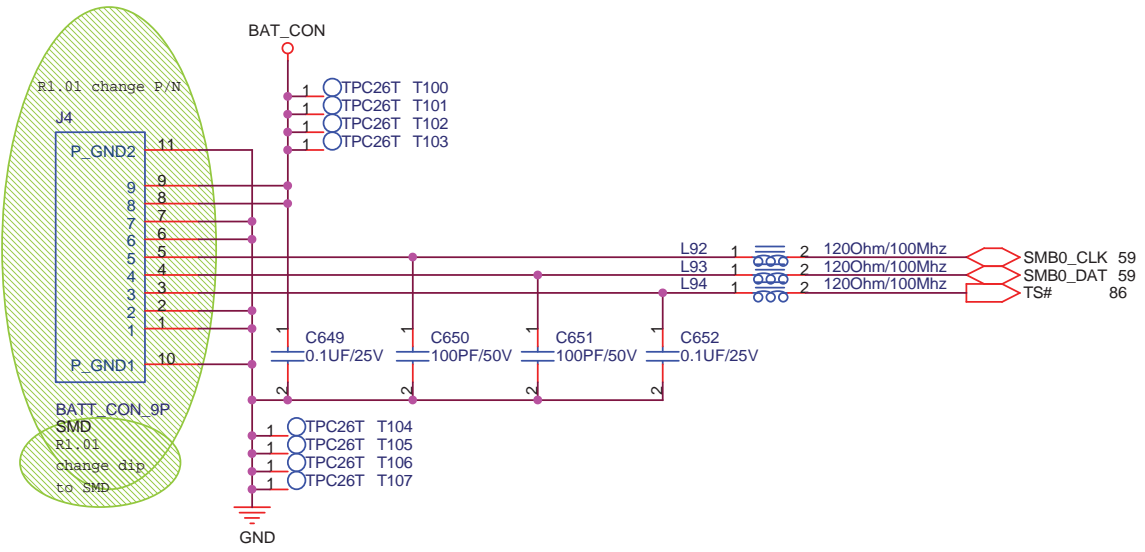
Sheet 67 of 92

DC IN

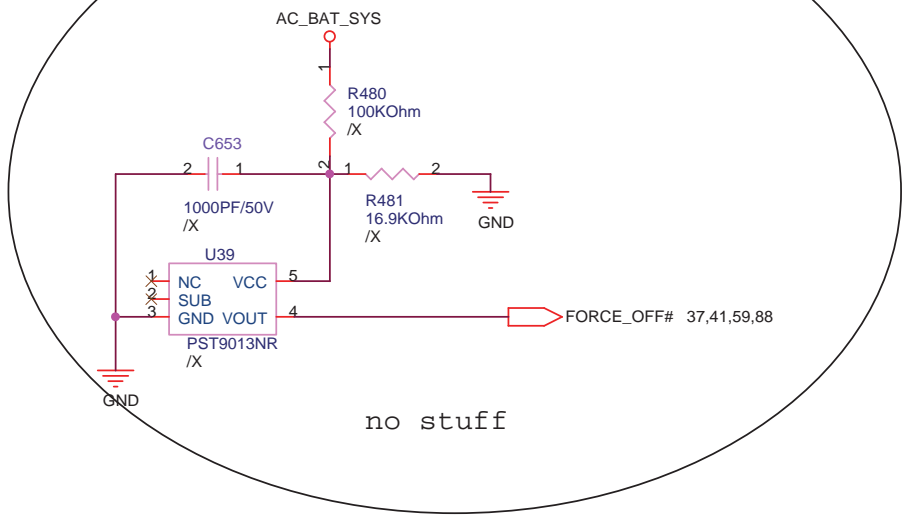


remove AC DC detect; no need

BAT IN



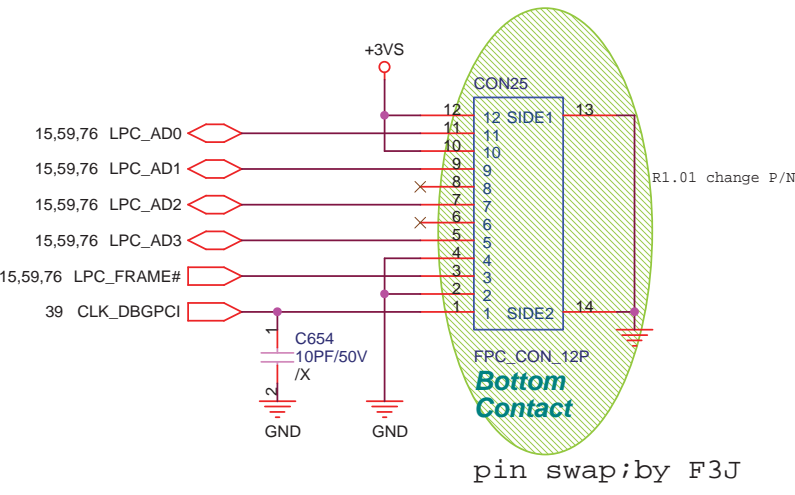
Without Battery & Pull out Adapter







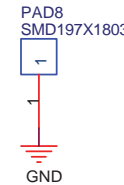
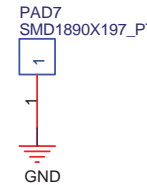
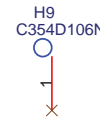
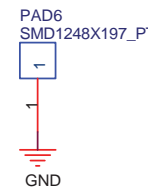
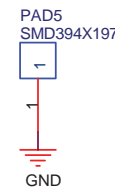
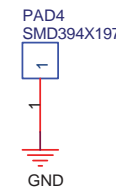
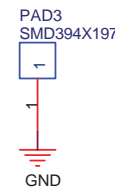
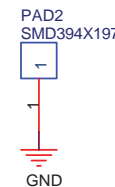
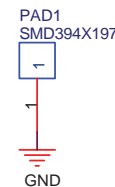
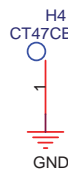
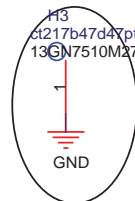
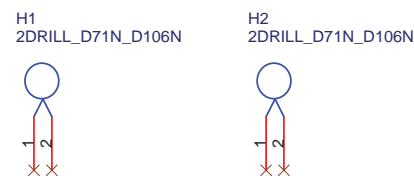
For Debug



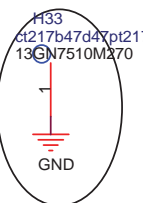
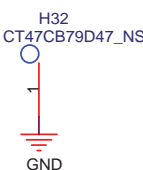
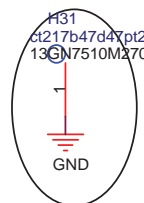
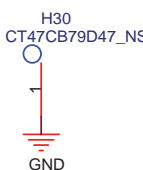
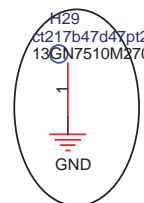




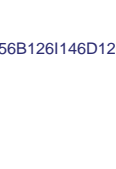
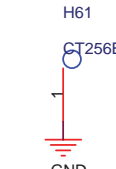
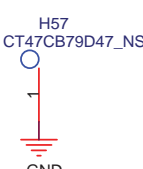
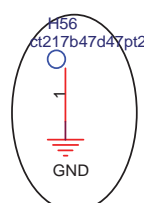
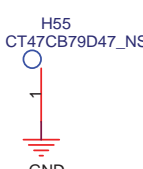
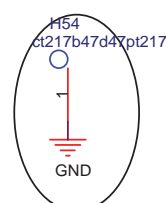
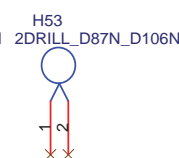
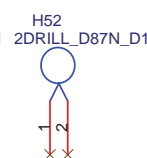
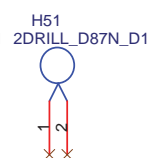
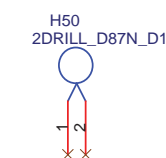
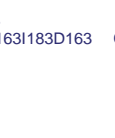
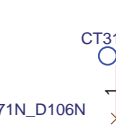
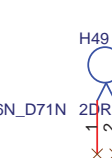
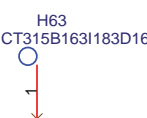
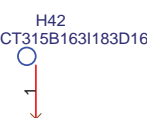
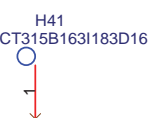
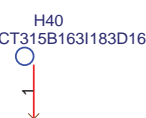
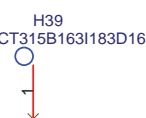
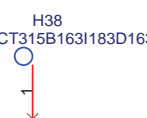
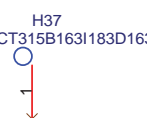
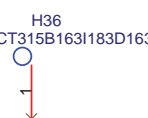
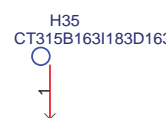
5					4					3					2					1				
D																								
C																								
B																								
A																								



FOR SCREW HOLE



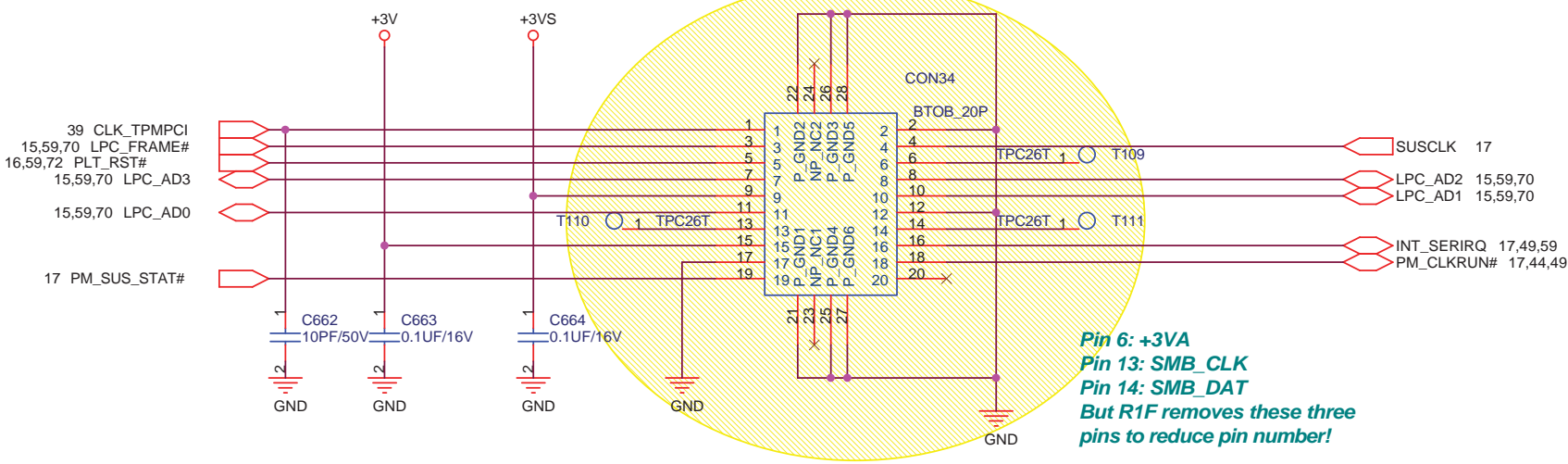
FOR SCREW HOLE

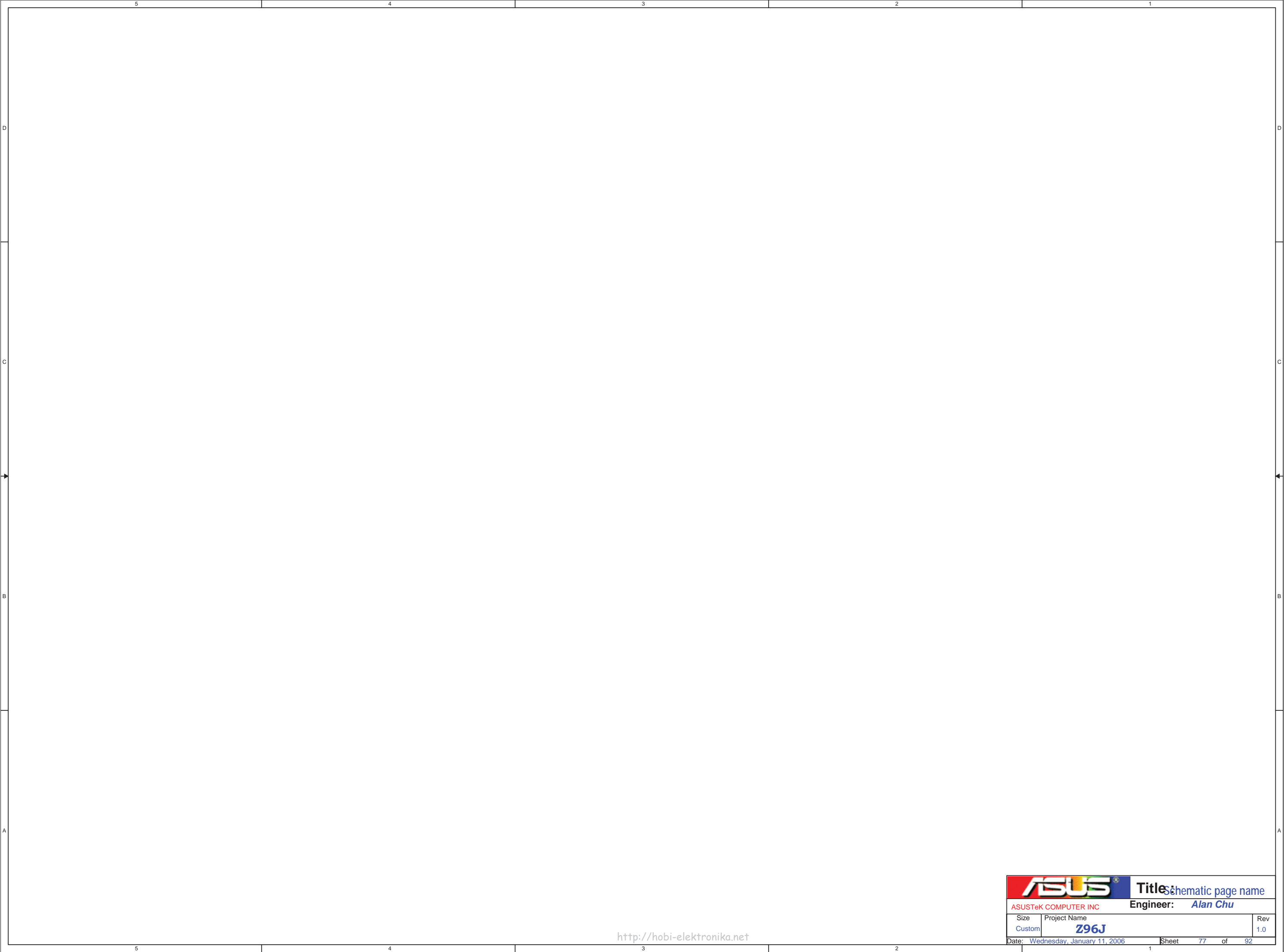






For TPM Module







**Title:** Schematic page name

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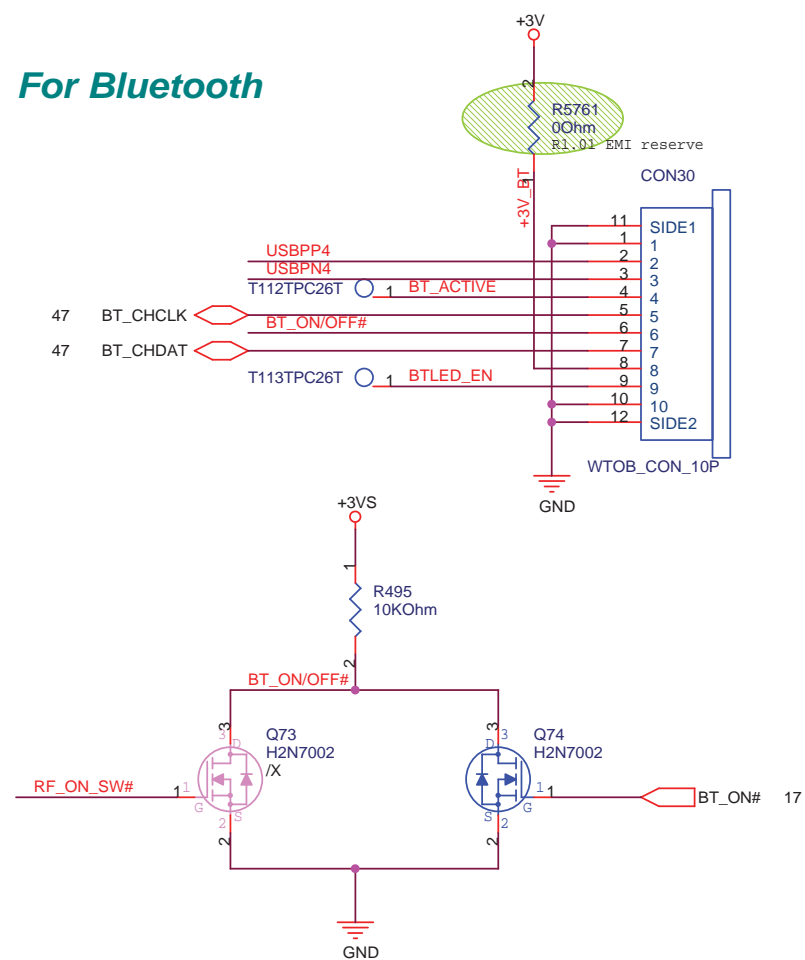
**Engineer:** Alan Chu

Size	Project Name	Rev
Custom	Z96J	1.0

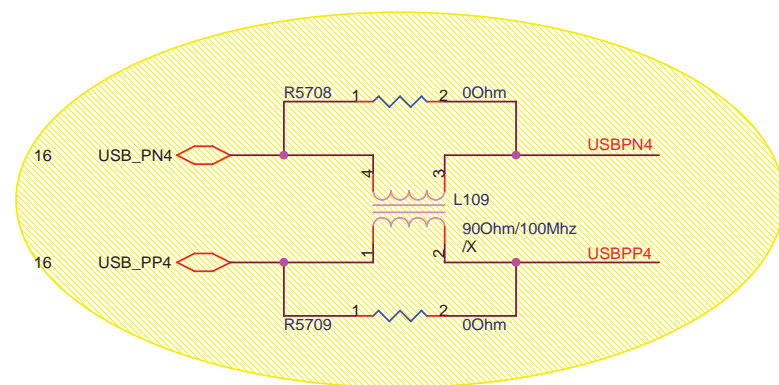
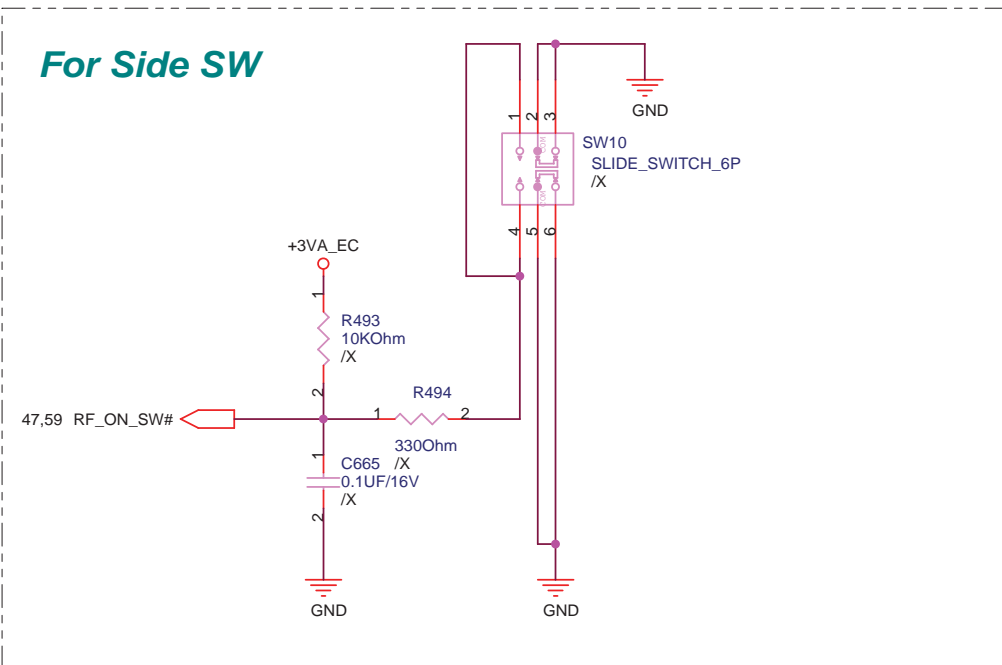
Date: Wednesday, January 11, 2006

Sheet 77 of 92

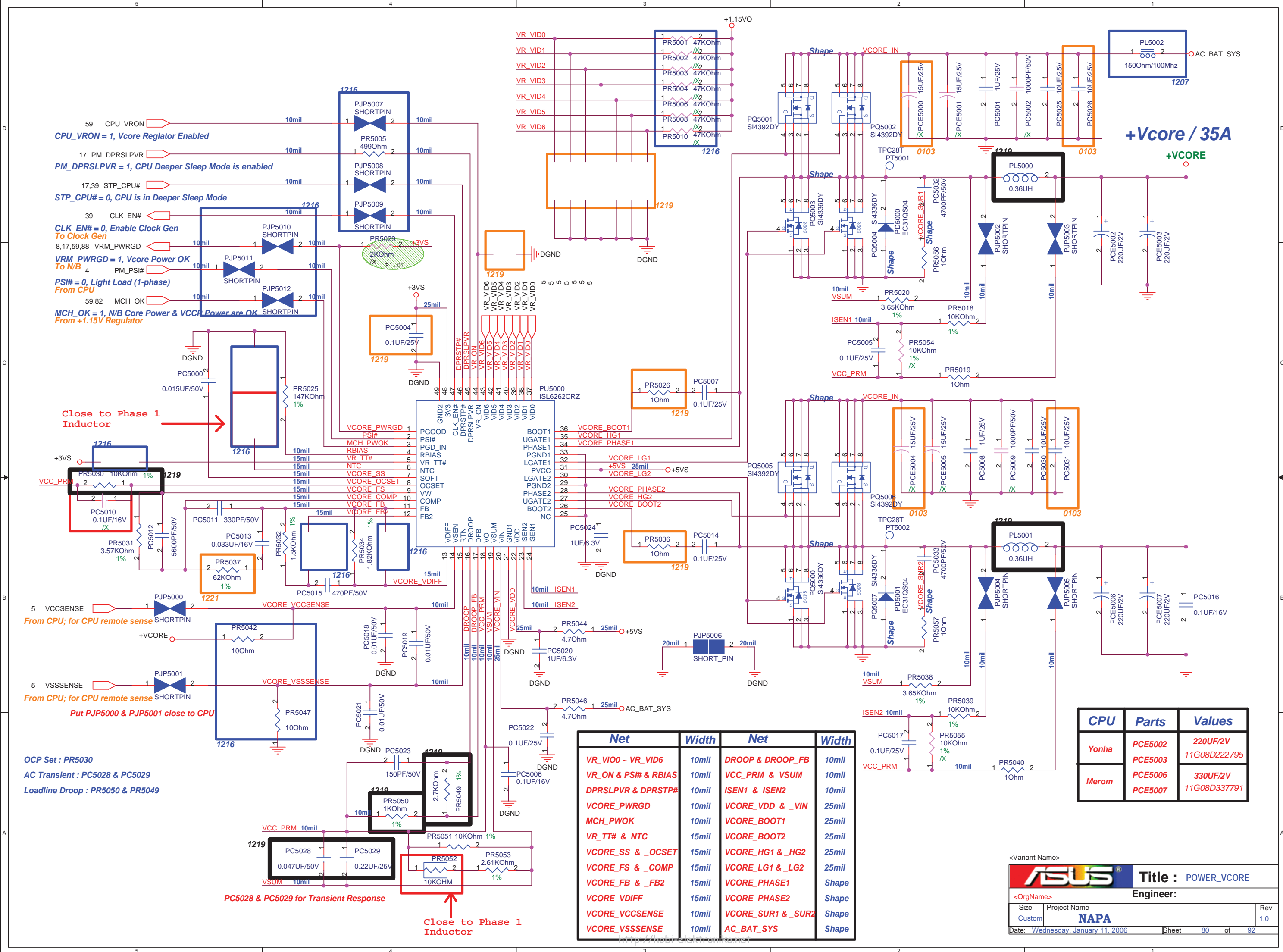
# For Bluetooth



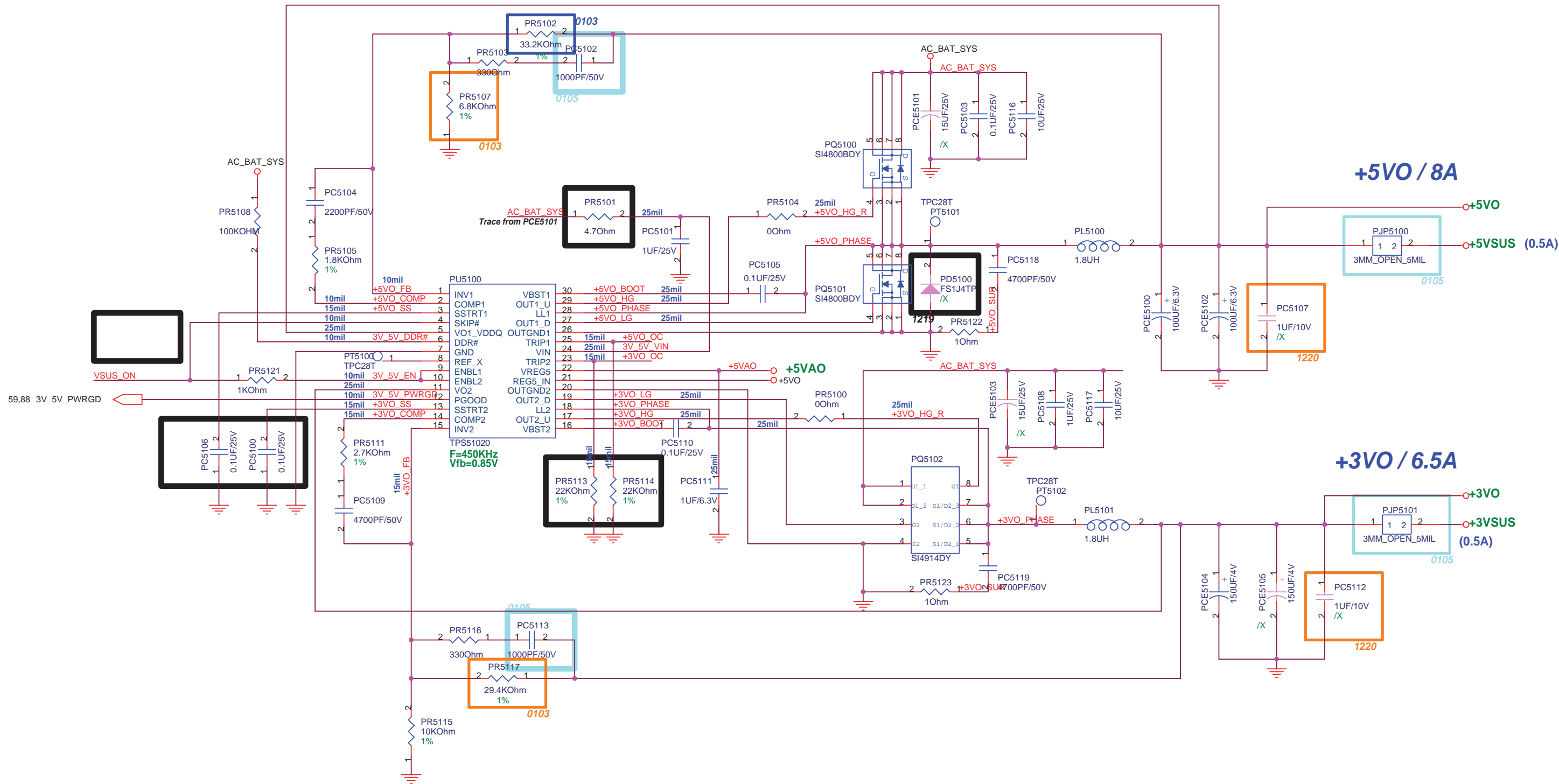
# For Side SW



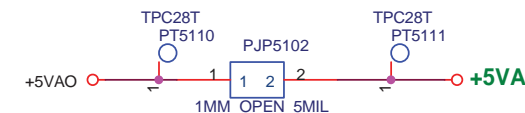
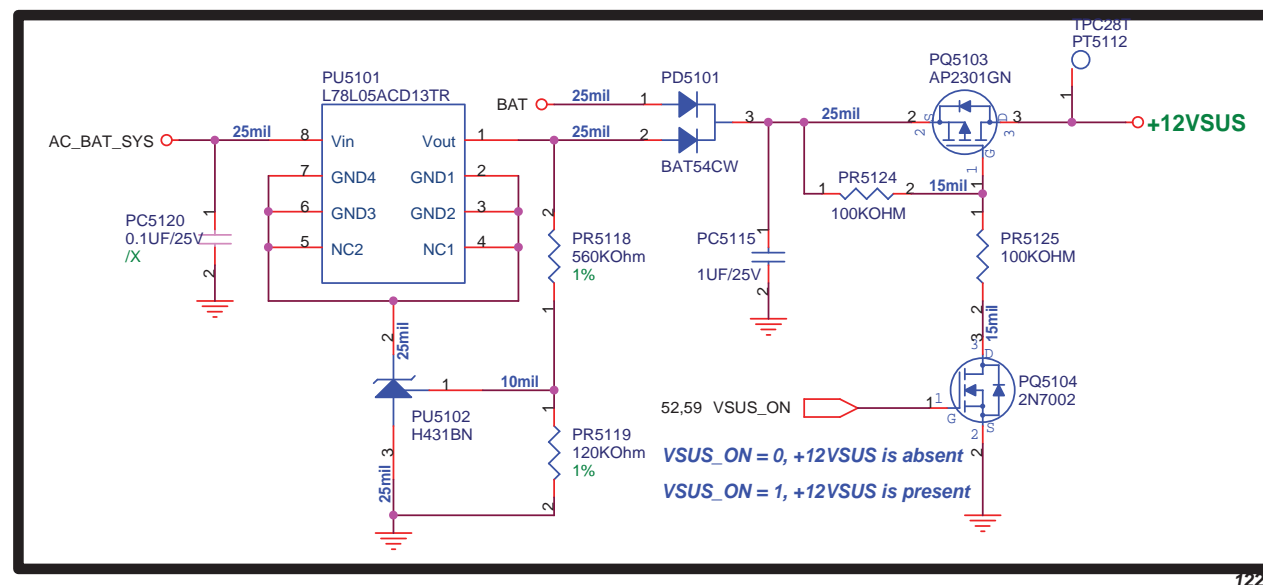


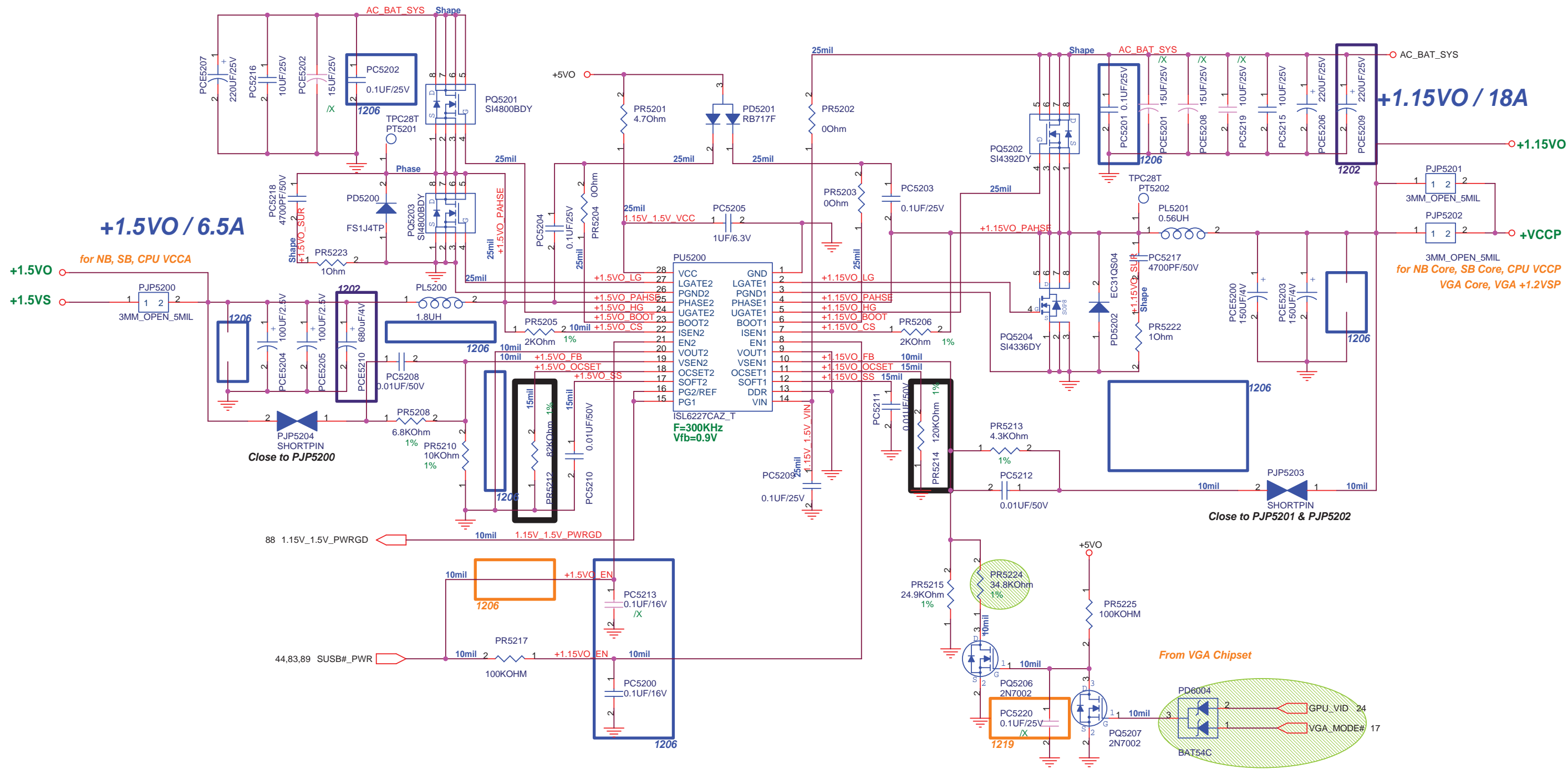






Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil





**+1.5VO / 6.5A**

**+1.15VO / 18A**

for NB, SB, CPU VCCA

for NB Core, SB Core, CPU VCCP

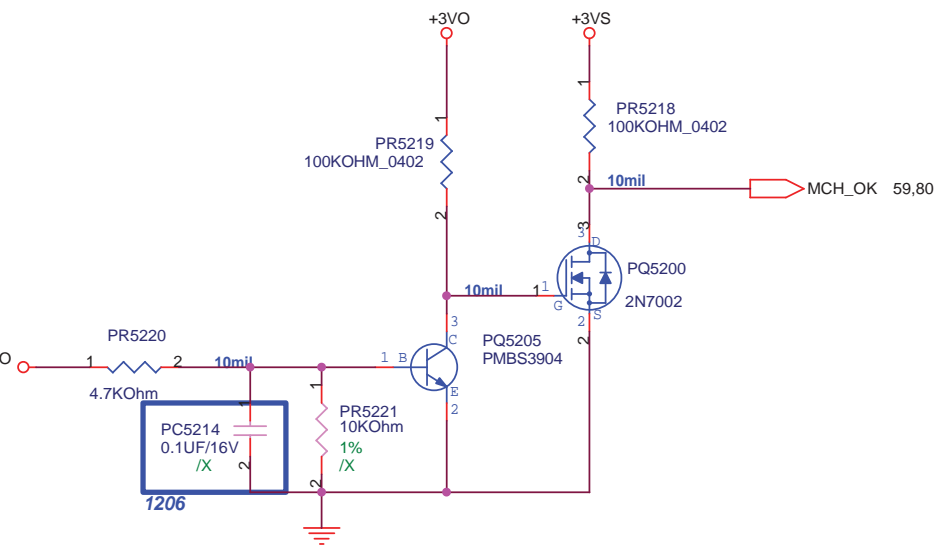
VGA Core, VGA +1.2VSP

Close to PJP5200

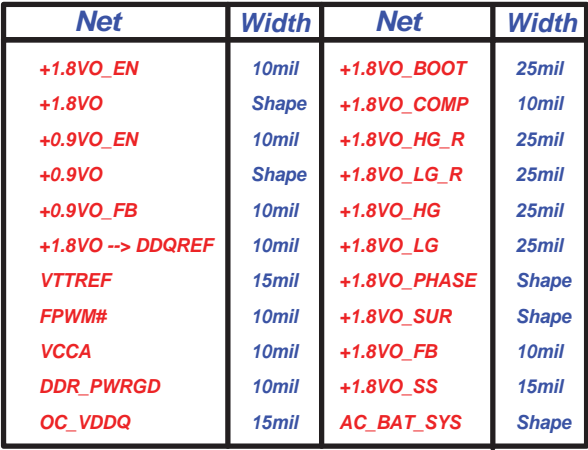
Close to PJP5201 & PJP5202

From VGA Chipset

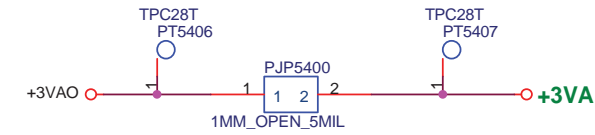
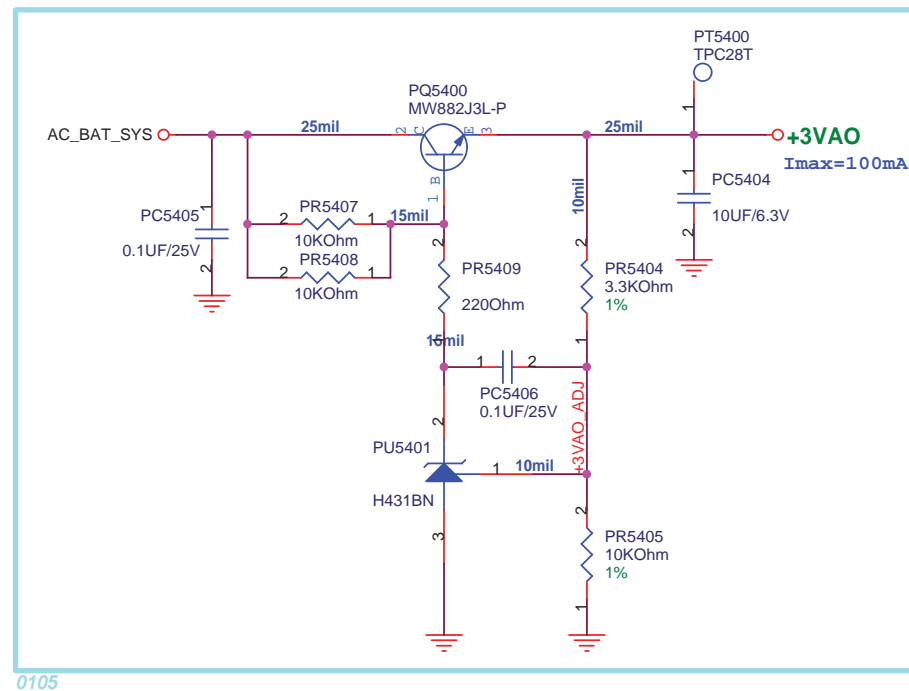
GPU\_VID = 1; Battery Mode ; +1.15VO = 1.055V  
GPU\_VID = 0; Performance Mode ; +1.15VO = 1.158V



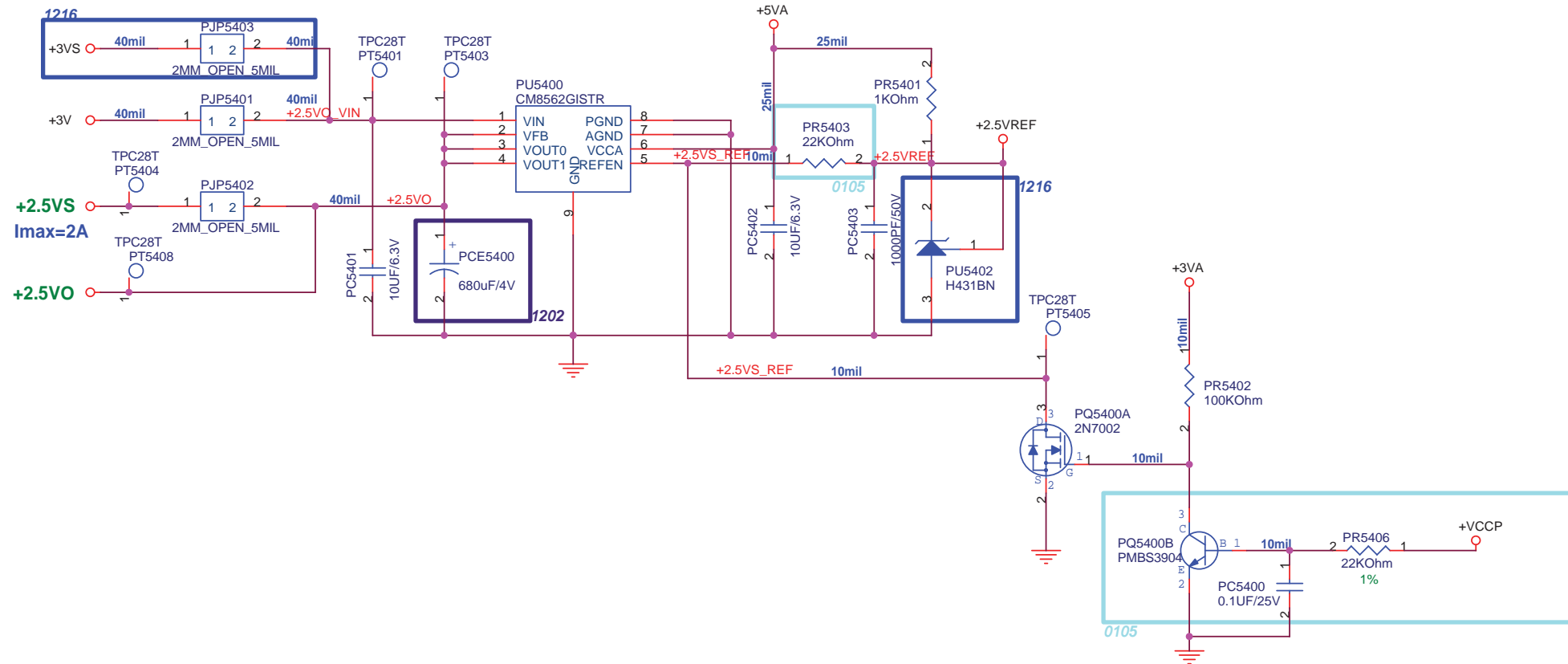
Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

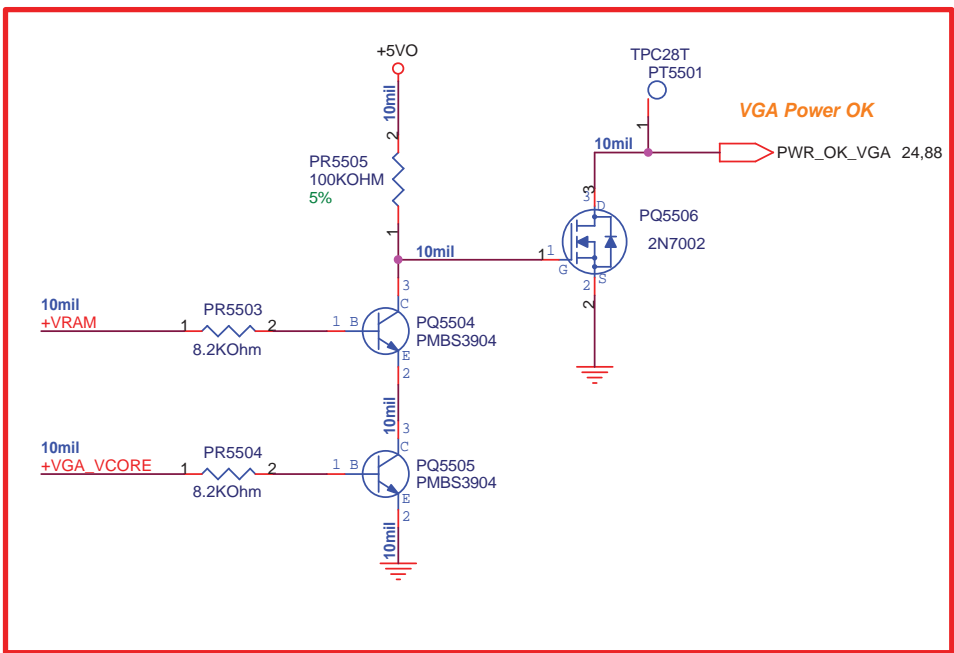
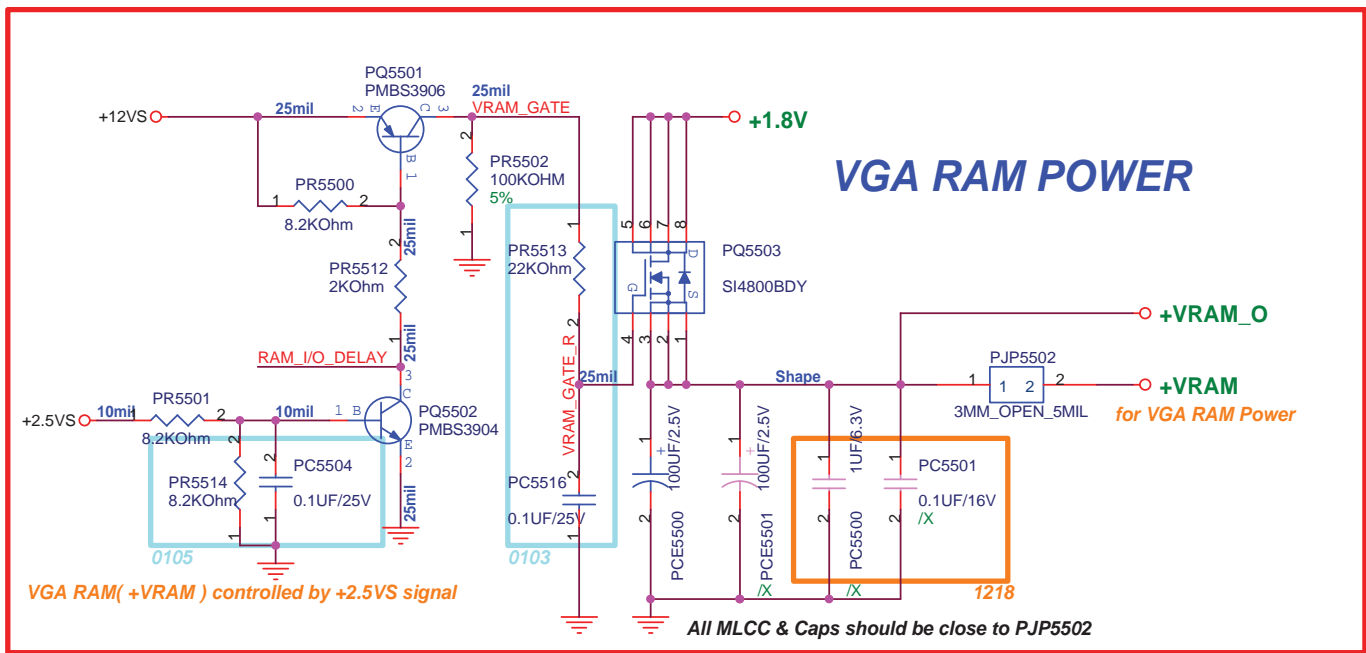


## +3VAO / 100mA

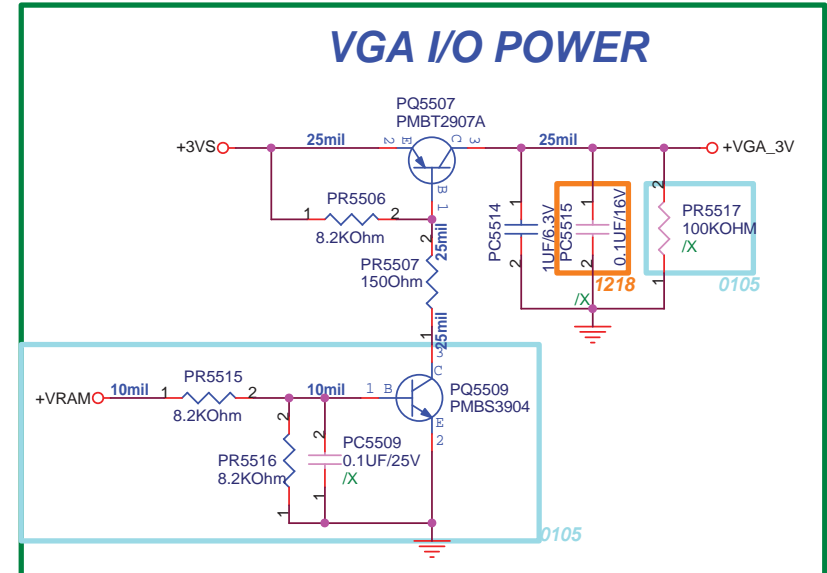
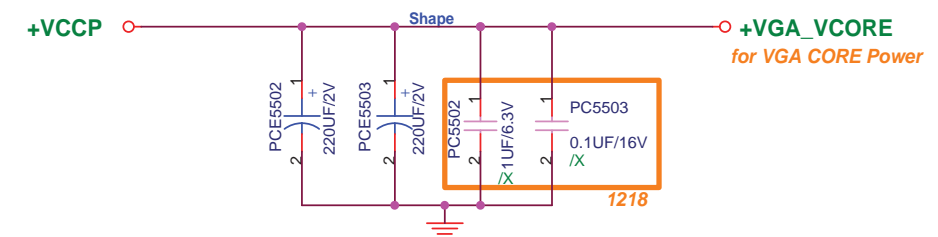


## +2.5VS / 2A



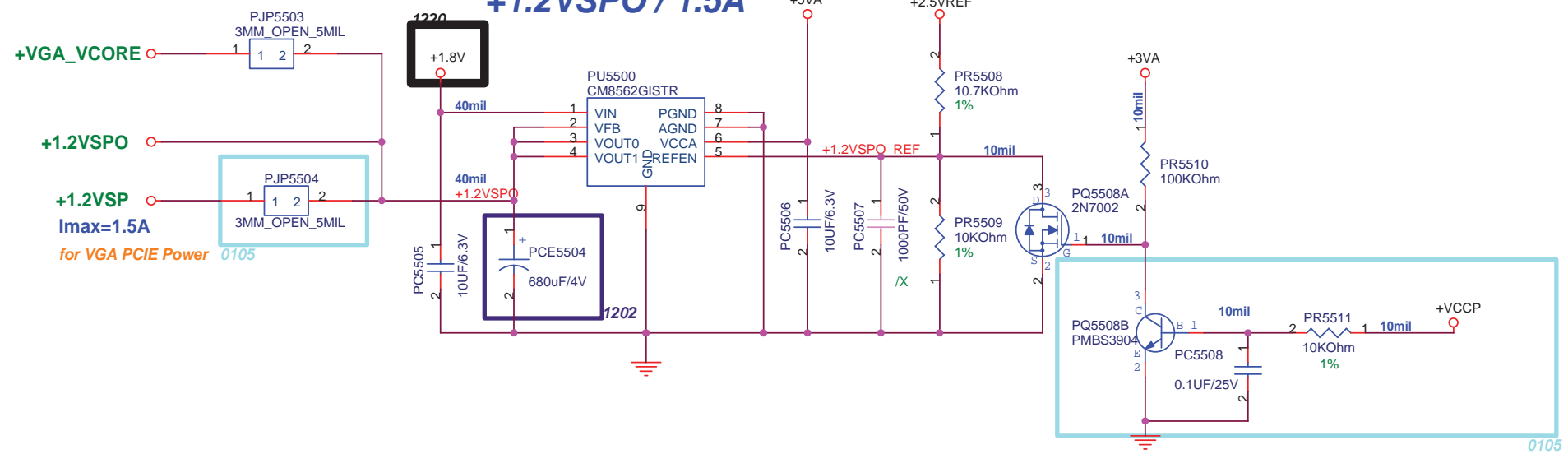


### VGA CORE POWER



### VGA PCI-E POWER

+1.2VSPO / 1.5A





## POWER PATH & BAT\_LEARN

AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN  
> 17.44V active

Adapter lin(max) =  $[0.075V/R_{sense}(A_{lin})] \cdot [V_{CLS}/V_{REF}]$   
 $R_{sense}(A_{lin}) = 0.02 \text{ ohm}$   
 $V_{CLS} = 3.685V$   
 $\Rightarrow \text{lin(max)} = 3.27A$   
 $\Rightarrow \text{Constant Power} = 19 \cdot 3.27 = 62.13W$   
 $\Rightarrow R_{5710} = 20K, R_{5715} = 137K$

Adapter  $I_{in(max)} = [0.075V/R_{sense}(A_{Din})] \cdot [V_{CLS}/V_{REF}]$   
 $V_{CLS} = 2.865V$   
 $\Rightarrow I_{in(max)} = 2.544A$   
 $\Rightarrow \text{Constant Power} = 19 \cdot 2.44 = 48.336W$   
 $\Rightarrow R_{5710} = 20K, R_{5715} = 42.2K$

Charge Current  $I_{chg} = [0.075V/R_{sense}(CHG)] \cdot [V_{ICTL}/3.6V]$   
 $R_{sense}(CHG) = 25m\ \Omega$   
 $V_{ICTL} = 3V \Rightarrow I_{chg} = 2.5A$   
 $V_{ICTL} = 1.68V \Rightarrow I_{chg} = 1.4A$

$$V_{batt} = Cell * \{ V_{ref} + [(V_{CTL} - 1.8V) / 9.52] \}$$
$$V_{CTL} = 1.588V$$
$$\Rightarrow V_{batt} = 4.2V$$

VICTL < 0.8V or DCIN < 7V -->Charger Disable

<b>MODE ( Pin7 )</b>	<b>Battery</b>
High ( >2.8V )	4-Cell
Low ( <0.8V )	3-Cell
High Impedance (1.6V<Vmoce<2V)	Battery Learn

MAX8725\_REF : 4.2235V  
MAX8725\_LDO : 5.4V

**Battery Charging Voltage :**

$$+V\_BAT = 4 \times [4.2235 + (V_{vct1} - 1.8) / 9.52]$$

**Battery Charging Current :**

$$I_{charge} = (0.075 / PR5706) \times (V_{ictl} / 3.6)$$

***Input Adaptor Max. Current Limit :***

$$I_{limit\_current} = (0.075 / PR5701) \times (V_{cls} / 4.2235)$$

### Pre-Charging Mode :

Precharging current = 163.9mA

$$V_{ictl} = 0.098V$$

### Battery Cell Selection :

BATSEL\_2P# = 1, 6 Cells; Vct1 = 1.678V Charging Current = 156mA

$$\Rightarrow I_{\text{charge}} = 2.331 \text{ A}$$

BATSEL\_2P# = 0, 9 Cells; Vct1 = 2.785V CHG\_EN# = 1, Charger Disabled

$$\Rightarrow I_{charge} = 3.868A$$

59 AC\_APR\_UC 

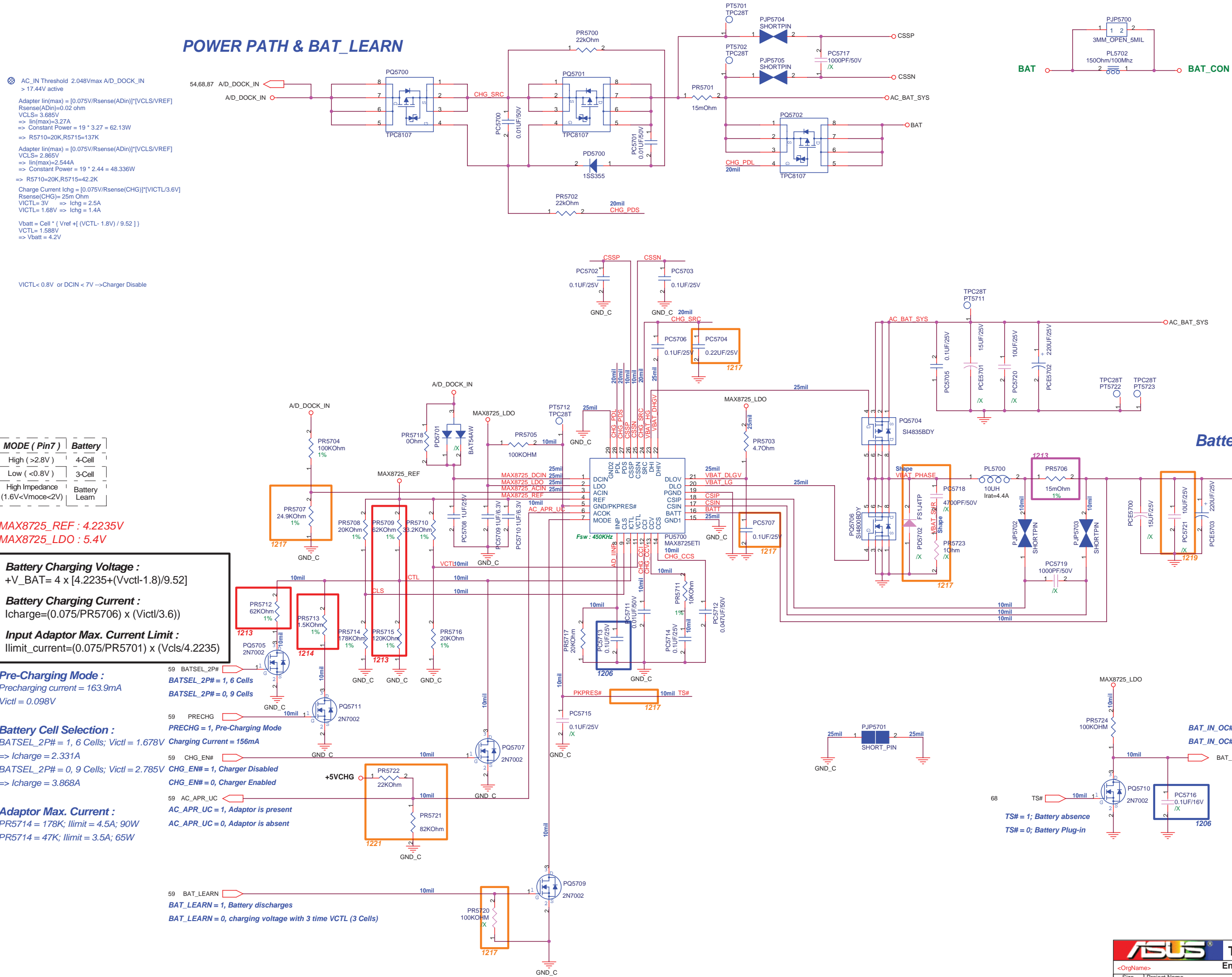
Adaptor Max. Cl

PR5714 = 178K:  $I_{limit} = 4.5A$ : 90W

PR5714 = 47K:  $I_{limit} = 3.5A$ : 65W $R_{S714} = 47\text{K}$ ,  $I_{lim} = 3.5\text{A}$ ,  $0.5\text{W}$ 

BAT\_LEARN = 1, Battery discharges  
BAT\_LEARN = 0, charging voltage

*BAT\_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)*



## Battery Voltage

*BAT\_IN\_OC# = 1; Battery absence*

*BAT\_IN\_OC# = 0; Battery Plug-in*

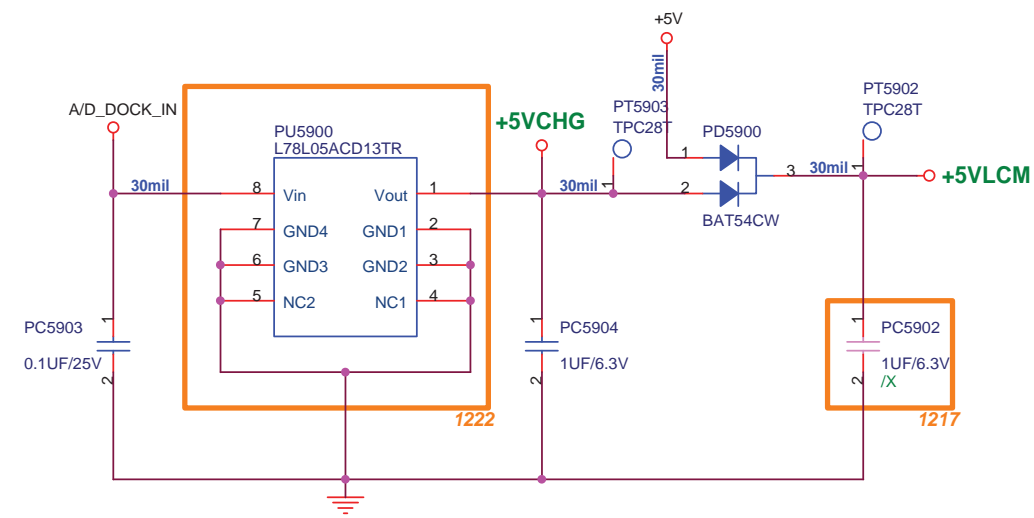
TS# = 1; Battery absence

TS# = 0; Battery Plug-in

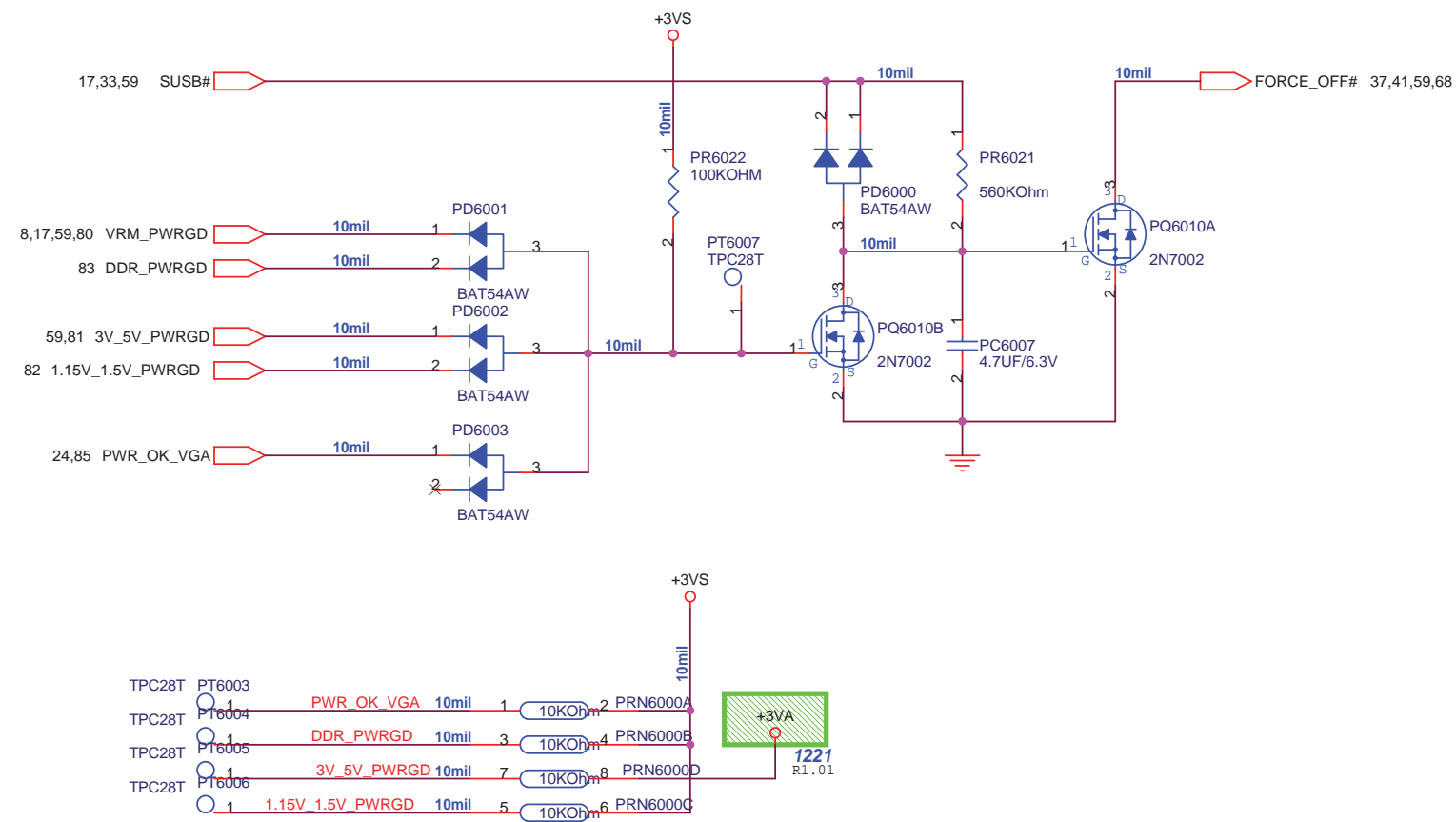


REMOVE BATTERY IN DETECT

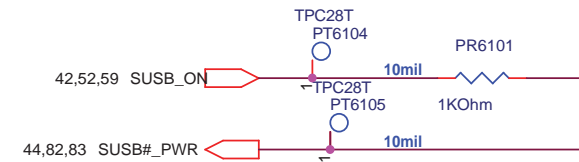
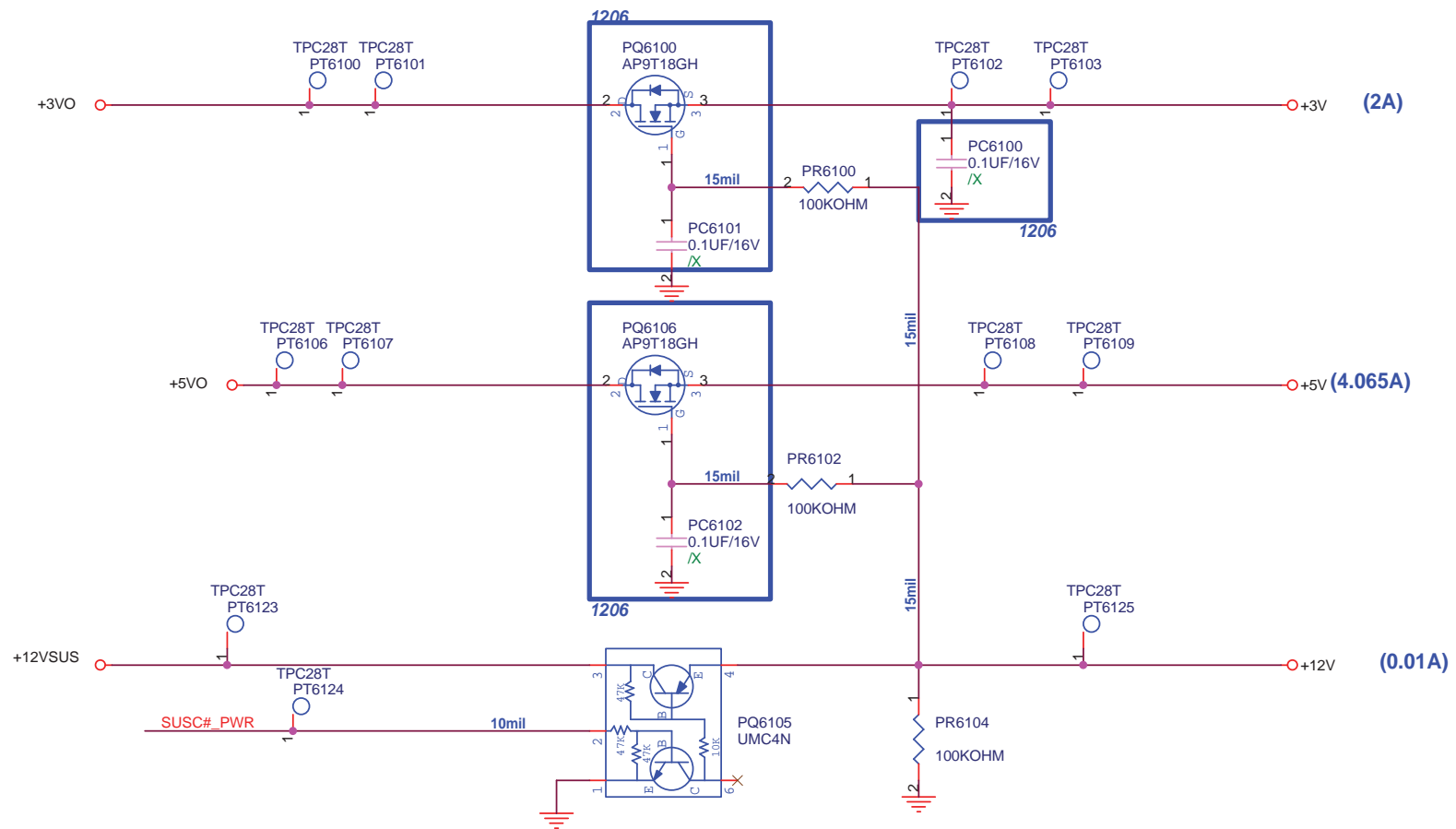
+5VLCM / +5VCHG



## Power Good Detector



**SUSC#\_PWR POWER**



## SUSB#\_PWR POWER

